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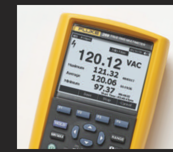

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DIFFERENT STROKES:

THE 34TH ANNUAL MICROPROCESSOR DIRECTORY

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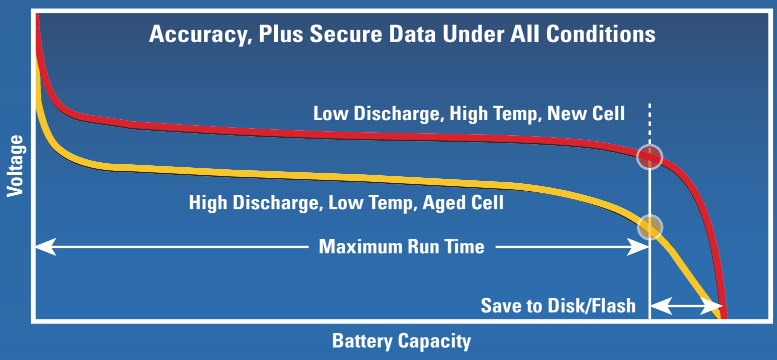

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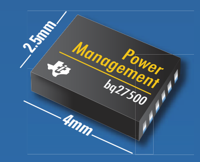

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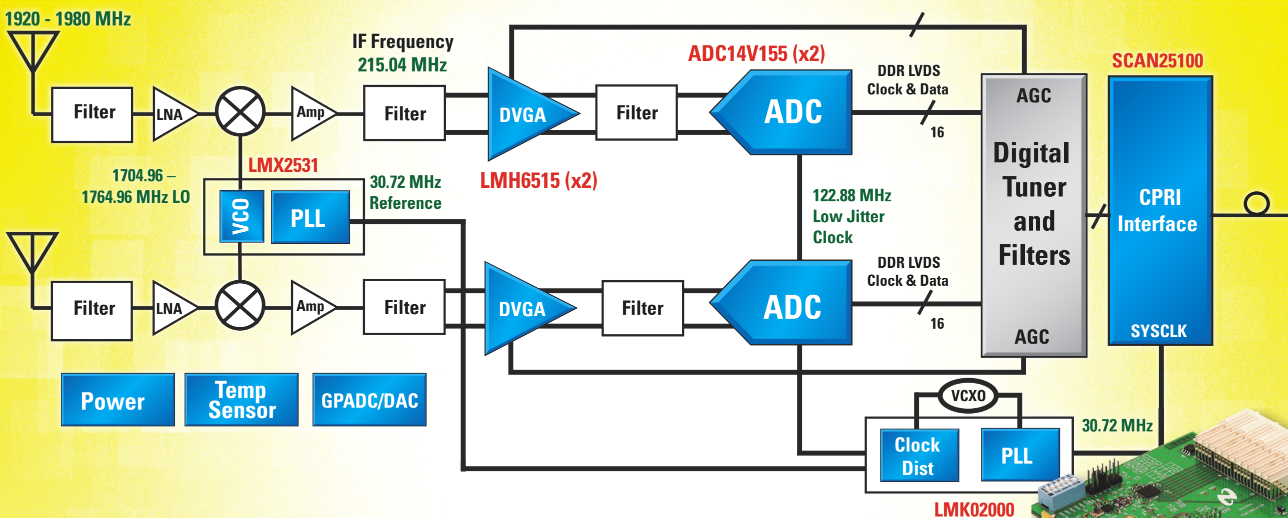

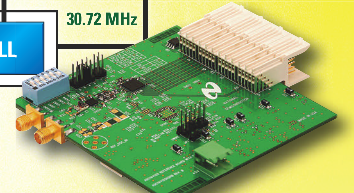

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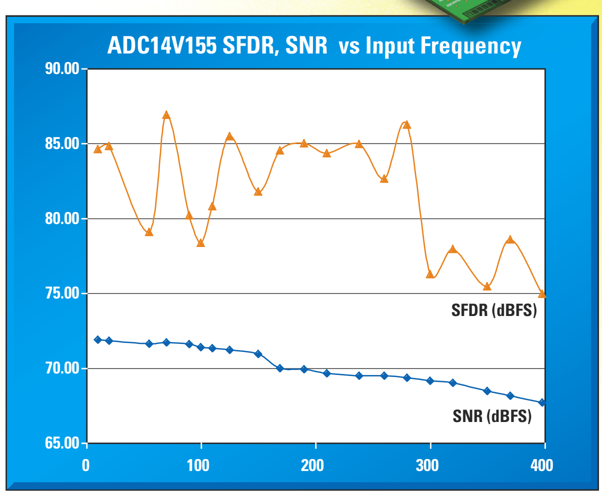

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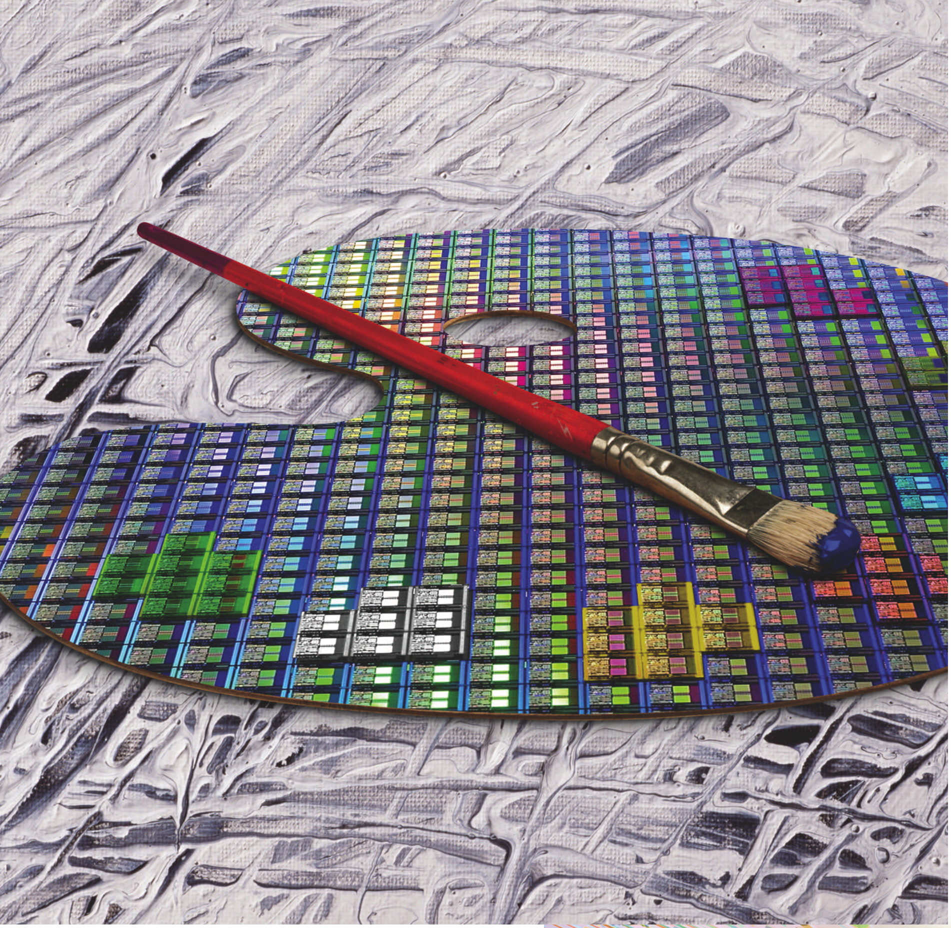

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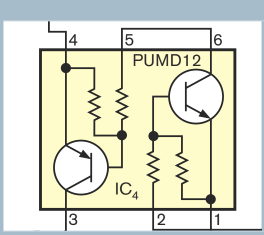

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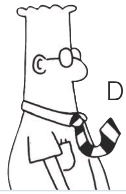

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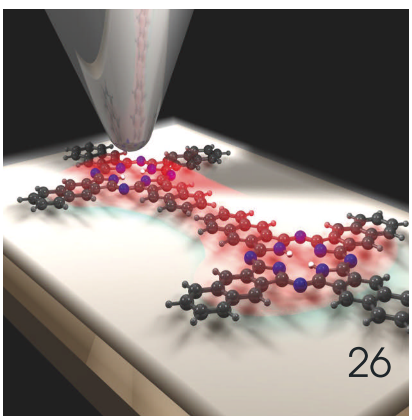

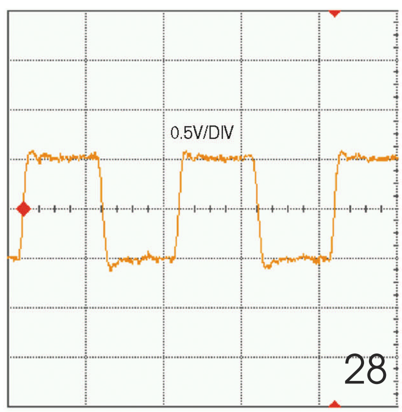

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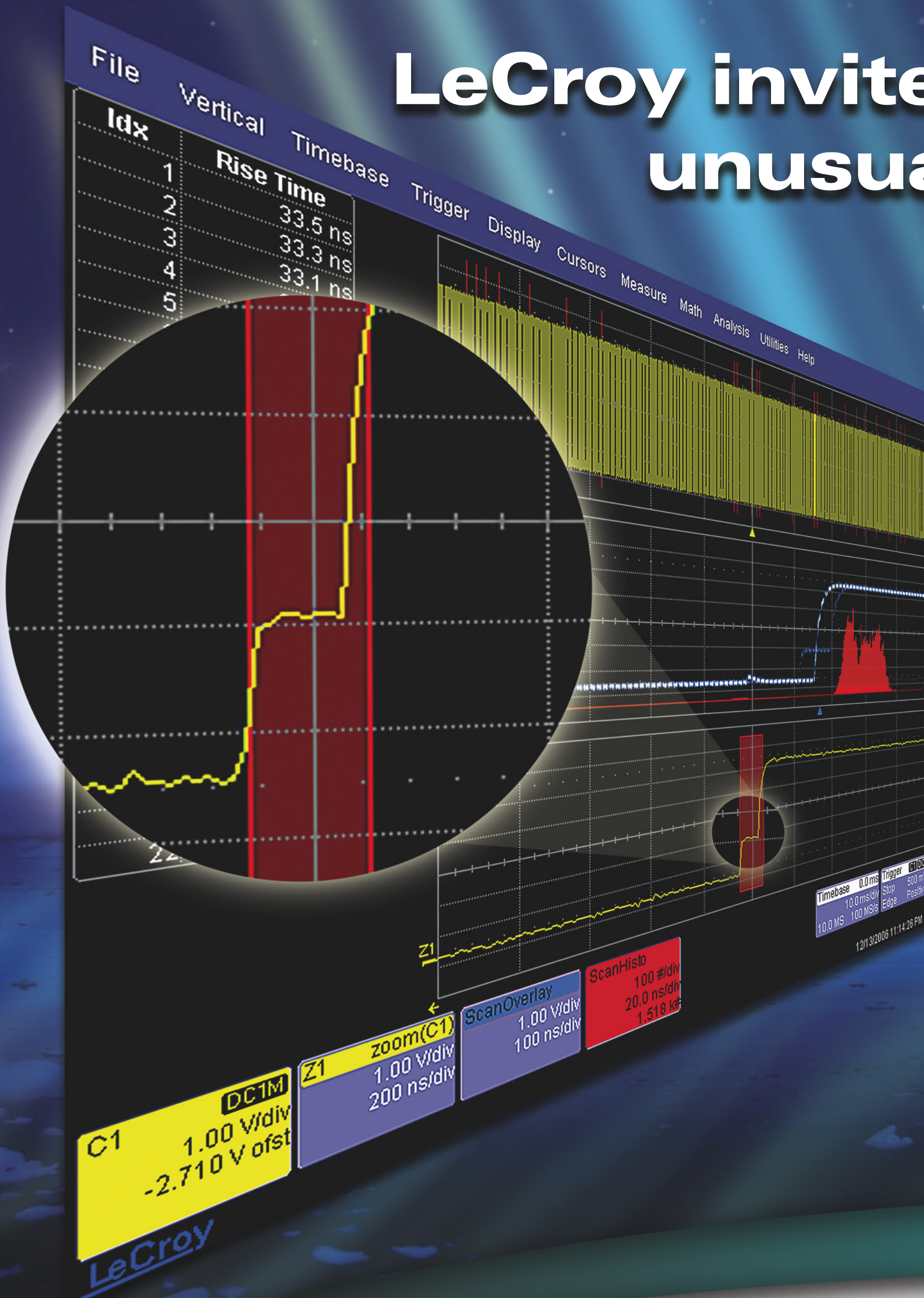

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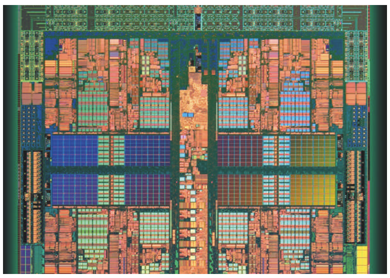

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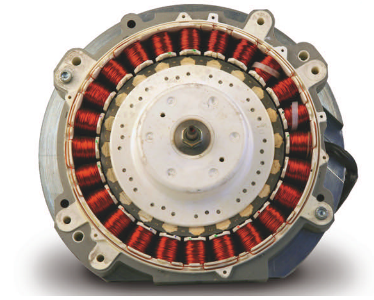

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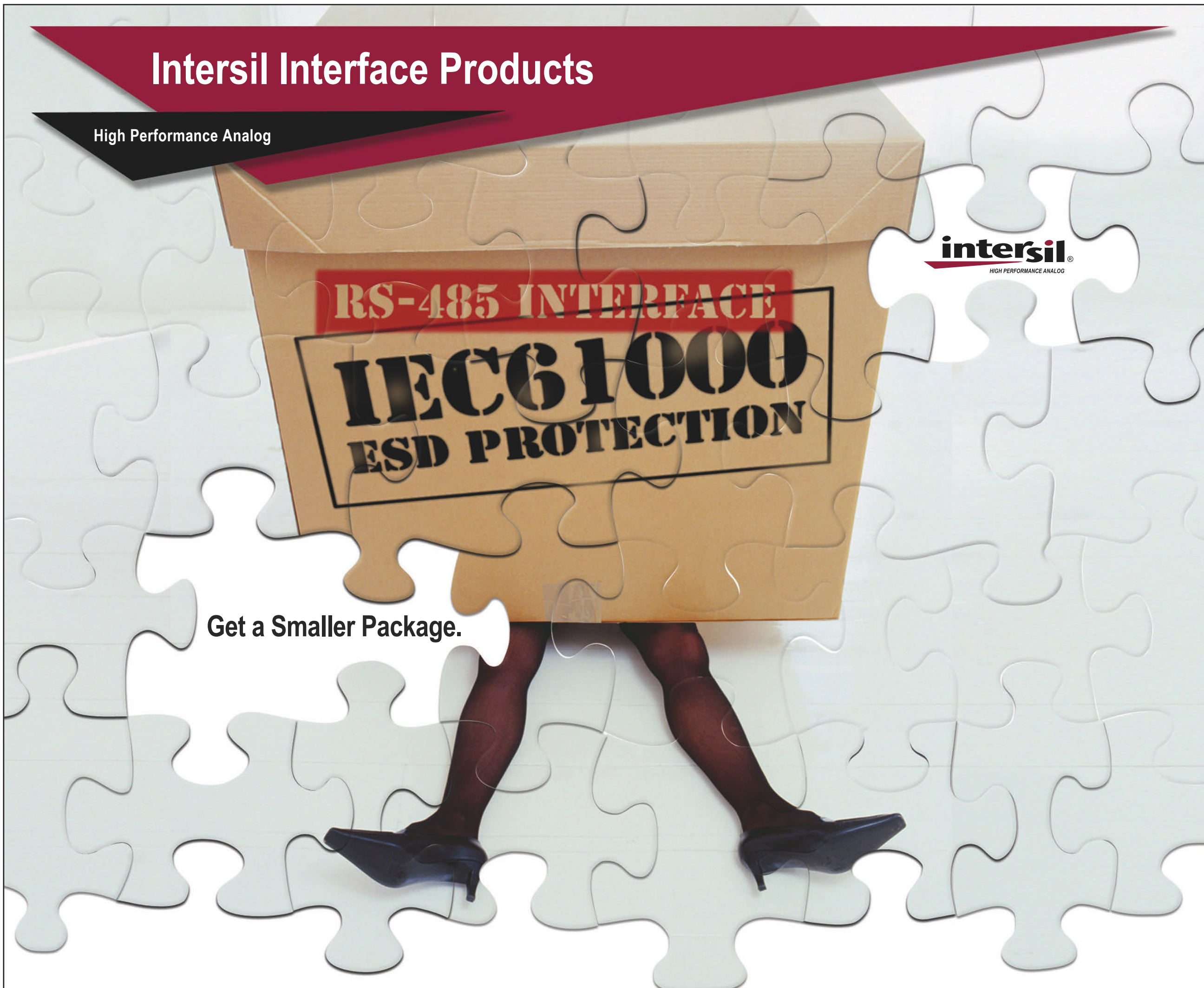

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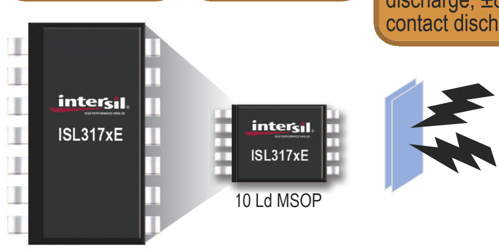

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ISL3172E	0.25	Yes	Yes	8 Ld MSOP, 8 Ld SOIC
ISL3173E	0.5	Yes	Yes	10 Ld MSOP, 14 Ld SOIC
ISL3174E	0.5	Yes	No	8 Ld MSOP, 8 Ld SOIC
ISL3175E	0.5	Yes	Yes	8 Ld MSOP, 8 Ld SOIC
ISL3176E	20	No	Yes	10 Ld MSOP, 14 Ld SOIC
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ISL3178E	20	No	Yes	8 Ld MSOP, 8 Ld SOIC

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BY MAURY WRIGHT, EDITORIAL DIRECTOR

Is municipal Wi-Fi a technical failure or a business failure?

I was a bit surprised recently to find the tech-centric article "Cities turning off plans for Wi-Fi" on the front page of a *USA Today* (www.usatoday.com/tech/wireless/2007-09-19-wifi_N.htm). That article echoed a number of other reports in the tech media about problems with municipal Wi-Fi projects. For instance, communication analyst Andrew Seybold has covered the topic in numerous blog posts and recently devoted an issue of his *Commentary* e-newsletter to the topic (www.andrewseybold.com/commentary.asp?ID=109). The consensus seems to be that deploying Wi-Fi in a mesh network that covers a significant amount of urban area is just too complex. But read between the lines, and you'll find that the message is that no one will pay for the service.

Wi-Fi certainly has technical limitations in a mesh deployment. The 2.4-GHz flavors have only three nonoverlapping channels. And as I've written repeatedly, Wi-Fi implementations don't come close to their specified range. But those technical issues aren't really behind the failure of municipal-Wi-Fi deployments. What is the problem? The cities and service providers behind the deployments completely misunderstand the potential user base.

Service providers targeting municipal Wi-Fi clearly expected to compete for customers with DSL (digital-subscriber-line) and cable-Internet service. And there is no way to deploy a wireless network that can compete costwise with the wired services when the wired infrastructure is already in place and paid for. Certainly, the urban areas targeted for municipal Wi-Fi are well-wired.

The cities and service providers behind the Wi-Fi deployments completely misunderstand the potential user base.

The potential user base for municipal Wi-Fi ranges from students to professionals that are on the move between meetings, classes, and other events. These users don't need municipal Wi-Fi as a primary Internet service but rather as a secondary, supplemental service.

The problem is that a number of Internet alternatives exist to buying a municipal-Wi-Fi subscription. Both the GSM (global-system-for-mobile)-communication and CDMA (code-division/multiple-access) camps are touting their cellular-based offerings. But Wi-Fi is also prevalent. In McDonalds and Starbucks, Wi-Fi is almost universally available.

EDN's IT organization has struck a deal with a coalition of Internet-service providers, and I can access service from most of the Wi-Fi service providers that operate in restaurants, bookstores, airports, and hotels. The service industry has now matured so that a user can buy a single subscription and get service in almost any urban area. If a municipal service were to succeed, it would require the operator to join such a coalition of service providers. The only exception that I see would be a city that simply wanted to serve citizens and businesses by footing the service bill. And, as the earlier-referenced articles mention, cities are unwilling to do so.

In the future, WiMax may be a better technical choice for high-speed urban wireless access than either Wi-Fi or the data-centric cellular offerings. But wide availability of truly usable WiMax-equipped notebook PCs is fairly far in the future if for no other reasons than power-consumption issues and lack of battery life. Last year, I tried the CDMA-centric EV-DO (evolution-data-optimized) service but wasn't enthralled with the performance. For now, I'll stick with the broadly available Wi-Fi services at restaurants and other businesses. The number of businesses offering such services grows daily.

Alas, the few municipal-Wi-Fi deployments that are operating reveal usability issues, as well. In a blog post in March, *EDN* Senior Technical Editor Brian Dipert wrote of some benchmark tests he ran with cellular connections and with the Google municipal deployment in the San Francisco Bay area (www.edn.com/071011b1). I don't know whether the Google Wi-Fi offering has improved of late, but, for any municipal-Wi-Fi service to succeed, it had better match the experience that the almost-ubiquitous wired coffee house offers. **EDN**

Contact me at mgwright@edn.com.


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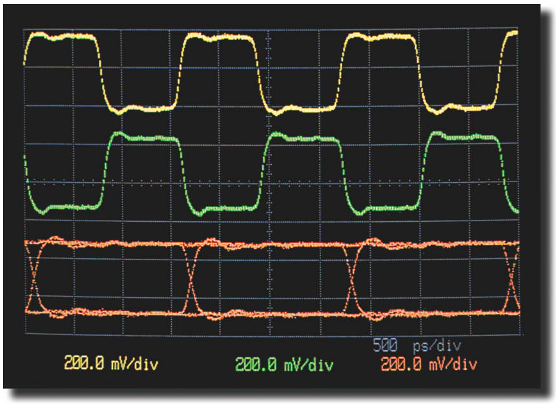
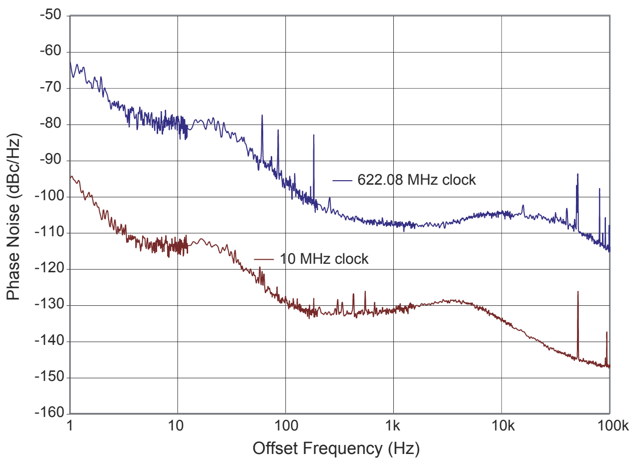


Clock and PRBS signals at 622.08 MHz

Plot shows complementary clock and PRBS (opt. 1) outputs at 622.08 Mb/s with LVDS levels. Traces have transition times of 80 ps and jitter less than 1 ps (rms).



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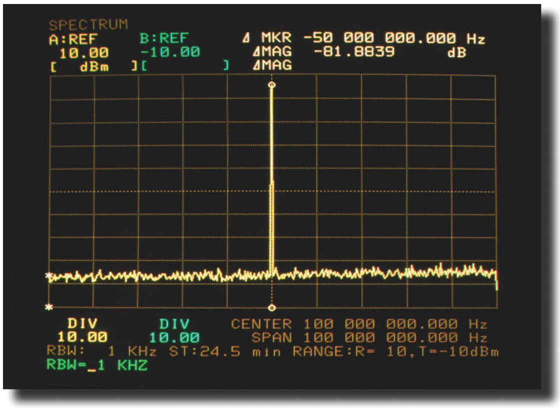

RF Spectrum of a 100 MHz clock

Graph shows a 100 MHz span around a 100 MHz clock. Only two features are present: the clock at 100 MHz, and the spectrum analyzer's noise floor (around –82 dBc).

Stanford Research Systems, Inc.

Phone: (408)744-9040
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ANALOG edge℠

High Speed ADC Input Driver Application Note

Application Note AN-1704

Hooman Hashemi, Applications Engineer

The LMH6555 differential amplifier is designed to drive the 100W differential input of GigaSample per second (GSPS) A/D Converters (ADCs) with up to 0.8 $V_{P\text{-}P}$, and to present constant 50Ω input impedance to the terminating cable to achieve the highest return loss. This amplifier can be used either as a single-ended input to differential output, or simply as a differential-input/output driver. The mostly widely used application is in DC- coupled (or wideband) applications where a single-ended input is to be sampled by a high-speed differential input ADC. Compared to balun transformers, which are often used to perform this function, the LMH6555 offers several advantages: Common Mode (CM) voltage can be set (needed for ADC DC coupling), the ability to provide voltage gain, it can be DC-coupled (Baluns must be AC-coupled), the output voltage swing is matched with inputs of GSPS ADCs, and there is higher input return-loss by maintaining 50Ω input impedance to ground over a wide frequency range, and better gain balance.

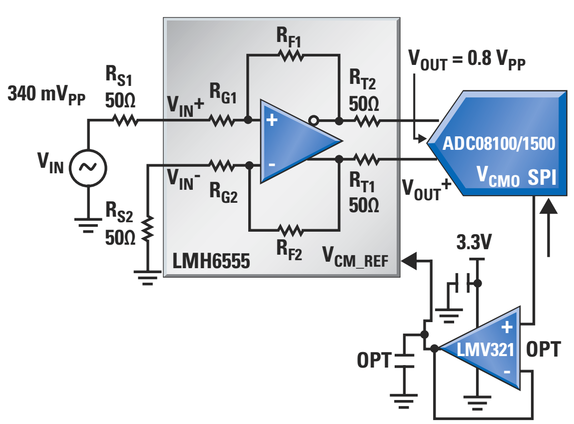

Figure 1. Active Single Ended to Differential Conversion for Broadband Applications

The LMH6555 spans the frequency range from DC up to 1.2 GHz (-3 dB bandwidth limit of the LMH6555). Accurate output CM voltage control is maintained by tying the V_{CMO} of the ADC to the V_{CM_REF} input of the LMH6555. This enables the capture of the full signal spectrum while the LMH6555 automatically maintains common mode control. The buffer (LMV321) shown in ***Figure 1*** boosts the current out of the ADC V_{CMO} pin so there is adequate drive for the V_{CM_REF} input. This buffer may or may not be needed, depending on the output current capability of the ADC. Most other commercially available drivers have a similar output CM control scheme, though the adjustment range of each is different and is closely related to the range of voltages expected by the intended ADC.

For AC-coupled applications, ADC inputs are internally biased and there is no need for common mode feedback control. For these applications, the ADC V_{CMO} is grounded and the ADC inputs are internally biased. The LMH6555 V_{CM_REF} pin needs to be biased to ~1.2V DC using a crude voltage divider from the 3.3V supply.

The LMH6555's gain (differential output to single ended input) is fixed at 4.7 V/V (see ***Figure 1***) where R_{S1}=R_{S2}=50Ω. This gain includes the loading of the ADC (100W in this case) onto the driver's 50Ω outputs. When the input signal is larger in amplitude, lower the LMH6555 insertion gain by increasing the value of R_{S2} and R_{S1}. These two resistors should always be equal in order to keep the input balance for low output offset. In ***Figure 2***, the gain of the LMH6555, which is at the receiving end of a 50Ω cable, is reduced using R_X and R_Y. By proper selection of component values, the input impedance to the LMH6555 circuitry (at J1) is kept at 50Ω to maintain impedance matching. For low output offset voltage, the LMH6555 architecture requires good matching between the equivalent external impedances looking to each input.

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The input/output swing relationship of the LMH6555 is shown in ***Equation 1***:

$$V_{OUT}(V_{P-P}) = V_{IN}(V_{P-P}) * [RF/ (2Rs + Rin\_diff)]$$

Equation 1

where RF= 430Ω and R_{IN}_diff= 78Ω and are LMH6555 specific values.

Rs is the equivalent resistance that each of the LMH6555 inputs sees to ground (assuming that they are equal to each other). Increasing Rs will reduce the gain. The ADC shown requires 0.8 V_{P-P} across inputs.

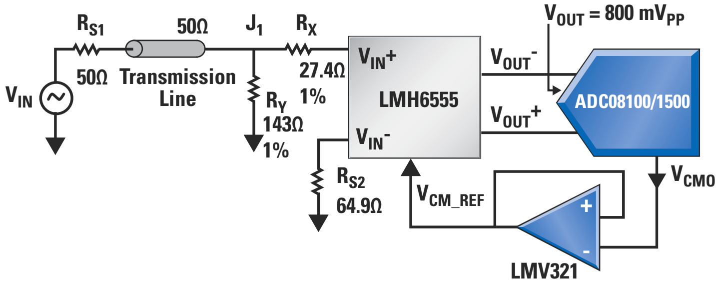

Figure 2. Setting the LMH6555 Gain while Maintaining Matched Input Impedance

Figure 2 is an example where the single- ended input is driven by a 50Ω transmission line that needs 50Ω to ground for proper termination. The series and shunt resistances, R_X and R_Y, present the proper cable termination (50Ω) and achieve the correct Thevenin resistance (64.5Ω) so that there is 0.8 V_{P-P} generated across the ADC inputs. In ***Equation 1***, "V_{IN} (V_{P-P})" would be the Thevenin equivalent voltage of the input network (R_{S1}, R_Y, and R_X) Thevenin equivalent resistance:

$$V_{Th} = 0.52V_{P-P} . R_Y/ (R_Y + R_{S1}) = 0.385V_{P-P}$$

$$R_{Th} = R_X + 1/ (1/R_{S1} + 1/R_Y) = 64.5Ω$$

You can use a spreadsheet to arrive at the proper values of R_X and R_Y in ***Figure 2***. Use "goal seek" find the value of R_X which would allow 0.8 V_{P-P} output swing. Similarly, R_Y can be adjusted for 50Ω input termination. Repeating this procedure will generate the resistor values needed. The LMH6555 maintains its low noise (19 nV/$\sqrt{Hz}$ output referred flat-band) irrespective of the R_S on its inputs because the input architecture is dominated by its equivalent input noise voltage and is independent of the source resistance.

Most amplifier-ADC interfaces require the use of series resistance and shunt capacitance in order to improve the transient response due to charge switching on the input of the ADC. In the case of the LMH6555 and its interface to National's ADC08xxxx family, the amplifier-ADC connection does not require this RC network because the LMH6555 has built-in series output resistances on each output to provide load isolation.

The ADC shown here requires that the CM voltage of the differential inputs be very close (within ±50 mV) to the V_{CMO} reference output it generates. This is one consequence of its 1.9V operating supply voltage because it constricts the voltage headroom of the ADC internal circuitry. If this CM operating condition is not maintained, the ADC full scale distortion performance will suffer.

Summary

Single ended to differential conversion of signals for interface to high-speed ADCs is a challenging task and should not be overlooked when high performance is required. This application note has examined some of the considerations and challenges of the input signal interface and has introduced one of the National's offerings (LMH6555) to alleviate this important task. Additional differential drivers intended for ADC interface include the LMH6550/51/52. ■

For Additional Design Information

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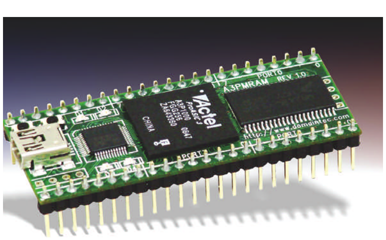
INNOVATIONS & INNOVATORS

FPGA-development card includes RAM, programmer

Claiming all the features necessary for developing reprogrammable-microcontroller applications, Domain Technologies recently announced a development card for Actel (www.actel.com) ProASIC3 FPGAs. Measuring only 2.4×1 in., the standard A3P-MRAM (magnetoresistive-random-access-memory)-1000 development card comes with an Actel A3P1000, 512 kbytes of 35-nsec nonvolatile MRAM, and an onboard device programmer. The high-speed MRAM device stores both programs and data, eliminating the need for flash-programming algorithms and boosting performance.

You perform all FPGA-device programming and software debugging of implemented microcontroller designs through the A3P-MRAM's built-in USB interface. The onboard device programmer is compatible with the STAPL (Standard Test and Programming Language) files generated by Actel's Libero integrated development environment. You use the same onboard device programmer and mini-B USB interface for accessing the A3P-MRAM's onboard JTAG emulator and debugger.



With built-in high-speed RAM and a device programmer, the A3P-MRAM-1000 offers designers a complete FPGA-development card in a 2.4×1-in. package.

The A3P-MRAM-1000 sells for $750 and is available from stock. For smaller development applications, Domain Technologies offers a lower cost version with an installed Actel A3P250. The A3P-MRAM-250 costs $640. The company ships each unit with stand-alone FPGA-device programming software and a mini-B USB cable.**—by Warren Webb**

▷**Domain Technologies**, www.domaintec.com.

FEEDBACK LOOP

"Sure, let's wheel that oxy-acetylene torch over here and unsolder the PCB. ... And the engineer was nitpicking about leakage in an LED-drive application? Duhhhh."

—reader and Design Idea contributor Glen Chenier does some nitpicking of his own. Read more about it in *EDN*'s Feedback Loop at www.edn.com/article/CA6466205.

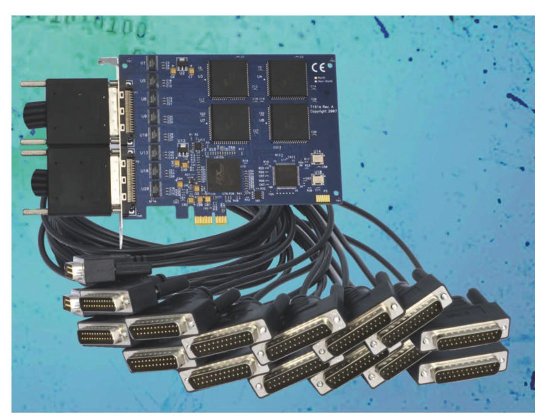
PCI Express board features 16 serial ports

With programmable-logic controllers, bar-code readers, scales, and similar data-acquisition and -control applications in mind, Sealevel Systems recently introduced the Comm+16.PCIe (Peripheral Component Interconnect Express), the first PCIe serial-I/O adapter with 16 high-speed RS-232 ports. Each serial port provides a maximum data rate of 460.8 kbps; 16C854 UARTs with 128-byte FIFOs drive the ports, providing error-free operation in high-speed applications. The module comes with a 16-port fan-out cable with standard DB-25M or optional DB-9M connectors.

The Comm+16.PCIe has an operating range of 0 to 70°C and, like all Sealevel I/O products, a lifetime warranty. The product includes SeaCom software support for the Windows 98, ME, NT, 2000, XP, and Vista and the Linux operating systems. Customers also receive the WinSSD software application for bit-error-rate testing, throughput monitoring, loop-back tests, and test-pattern-message generation. The standard price for the Comm+16.PCIe is $679, and it is now available.

—by Warren Webb

▷**Sealevel Systems Inc**, www.sealevel.com.



The Comm+16.PCIe is the first PCIe serial-I/O adapter with 16 high-speed RS-232 ports and a maximum data rate of 460.8 kbps.

AWR's new EM simulator touts flexibility

You don't usually associate the word "flexibility" with an EM (electromagnetic)-analysis tool, but the folks at AWR (Applied Wave Research) want to change that perception with the introduction of the Axiem EM-analysis tool. Axiem targets designers doing 3-D planar applications, such as RF PCBs (printed-circuit boards) and modules, LTCC (low-temperature-co-fired-ceramic) packages, MMICs (monolithic-microwave integrated circuits), and RF-IC designs. The tool will compete with EM solvers from Ansoft (www.ansoft.com), Eesof from Agilent (www.agilent.com), and others.

According to Sherry Hess, product-marketing manager at AWR, EM-analysis tools, even AWR's own legacy EM simulator, EMSPICE, which the company continues to support, have traditionally fallen into one of two bins: either accurate but slow or inaccurate but speedy and with low dynamic range. Most designers encounter design projects that require the positive attributes of both types of EM analyzers. Because no EM tool until now was both blazingly fast and accurate, these designers often had to buy both types of tools. Axiem eliminates this need because it allows users to tune its runtimes and accuracy to suit their needs. The speedup is so significant, Hess claims, that users will find it useful for both design and postdesign analysis.

To suit the tool for growing design complexities, AWR outfitted it with a new hybrid-meshing-solver technology and built the tool from the ground up to run on multicore-processing platforms. "Axiem is 'open-boundary,'" says Hess. "It has hybrid meshing, is extremely flexible, and will grow and expand as changes in IC and PCB modules take place. The more complicated designs get, the more designers will need the technology."

Traditionally, fast EM-analysis tools employ solvers based on a Sommerfeld integral equation to speed analysis, but the speed increase often comes at the expense of accuracy and dynamic range, scaling up runtimes by a factor of three as design complexity increases. Axiem's solver employs a fast multipole method that the company has tweaked for full-wave analysis. This approach essentially allows the tool to scale runtimes even faster as design complexity increases, maintaining accuracy, and run analysis faster than older tools.

> "Axiem's solver employs a fast multipole method that the company has tweaked for full-wave analysis.

To perform EM analysis, tools traditionally divide a structure into smaller areas with meshes of rectilinear shapes and then analyze those shapes and their relationships. But microwave and RF designs often include nonrectilinear structures, such as spiral inductors, that are difficult to mesh and analyze. To combat this problem, EM-tool vendors have introduced tools that use a triangular mesh, which increases accuracy but lengthens runtimes. To get the best of both worlds, the hybrid-mesh system automatically assigns rectilinear mesh to regular structures or regular parts of an irregular design feature and triangular mesh to any unique features, thus optimizing the runtime and accuracy of a simulation run. The tool automatically tweaks which features receive a rectilinear mesh and which receive a triangular mesh. The tool's meshing can also handle the increasing thickness and the width-to-height ratio of conductors in newer process geometries, accounting for silicon irregularities on the X, Y, and Z axes.

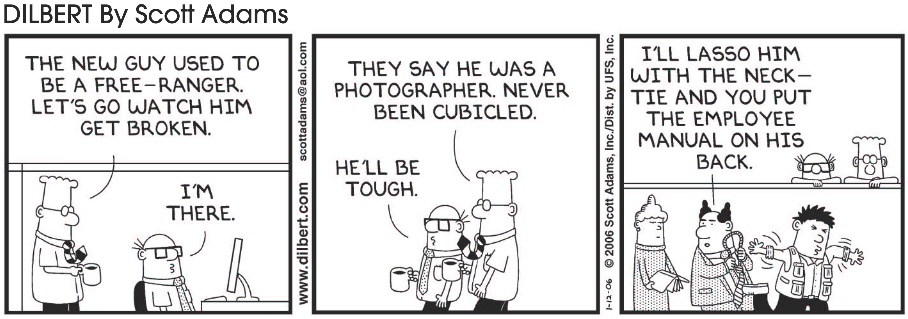
"With high-frequency effects, you typically have a lot of the information you have to capture before you can do additional circuit simulation and harmonic-balance simulation, and it has to be accurate down to dc," says Hess. "Our simulator spans dc. You don't have to do a dc simulation, then do high-frequency analysis, and then mathematically stitch these two together. The solver spans the full range."

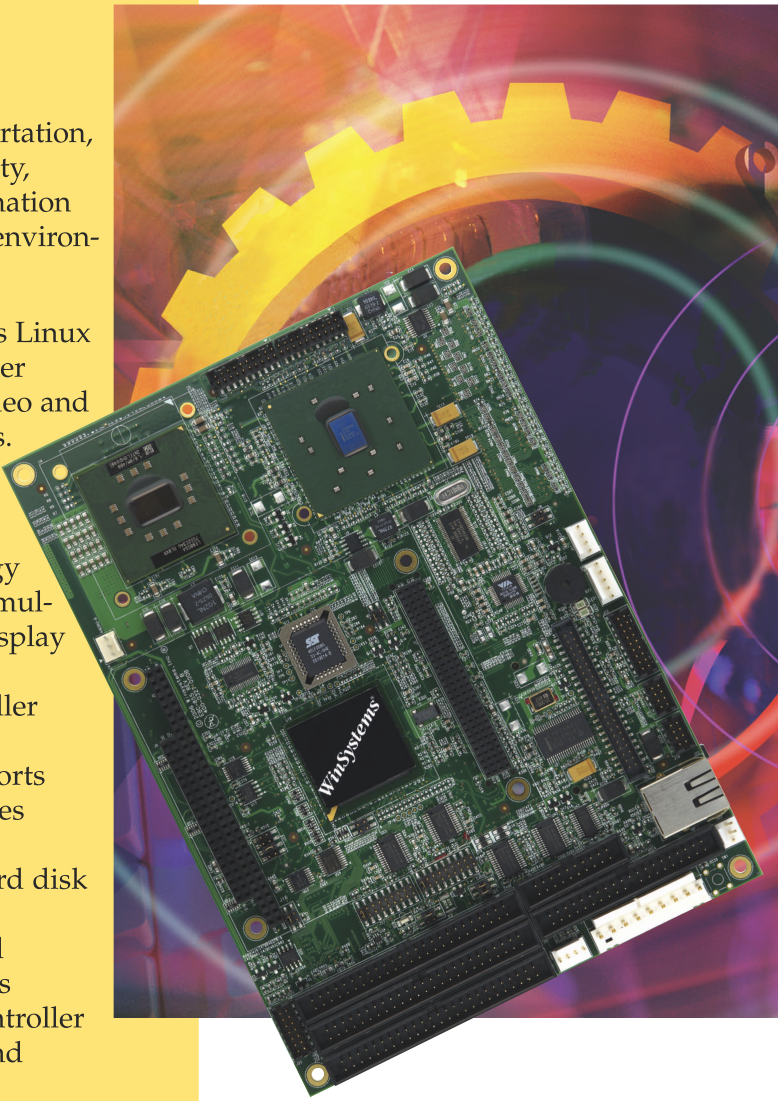
The tool takes advantage of computer systems employing multicore-processing technology, targeting use in quad-core processors. It also ties into AWR's Ace technology, in which all AWR tools run from a single data model, allowing all the tools in the AWR lineup to share design data. The tool links through Ace into OpenAccess so that it can share data with other third-party tools using OpenAccess. The company has not released any metrics of runtime because the tool is still in beta production, but the company expects to have more data on the tool's performance in the coming months. AWR plans to release the tool for mass distribution by the first quarter of next year. The price for a single-user, node-locked, perpetual license, running on Microsoft operating systems, starts at $30,000.

—by Michael Santarini

▷**Applied Wave Research**, www.appwave.com.

DILBERT By Scott Adams




WinSystems

10,000-count, handheld DMMs simplify installation and maintenance applications

Agilent Technologies is expanding its line of handheld DMMs (digital multimeters) with the announcement of the U1240A Series, which provides functions suiting installation and maintenance applications. The new DMMs allow engineers and field and facilities technicians to measure more than just voltage, current, and resistance. For instance, users can observe open- and closed-switch behaviors in the presence of intermittent signals and, with the DMMs' dual- and differential-temperature capabilities, can easily gauge refrigeration-system efficiency and the extent of transformer heating. Coupled with the microampere-measurement function, the dual-temperature-measurement capability is handy for troubleshooting HVAC (heating/ventilation/air-conditioning) equipment and sensors.

When maintaining ac motors or troubleshooting circuit breakers that trip prematurely, the U1240A Series helps users quickly verify the presence of harmonics that may have caused device overheating. With their internal memory, the DMMs let users conveniently collect data on the go for later analysis. "With the addition of the U1240A Series, we now offer a wider selection to fit customers' applications and budgets across electronics troubleshooting, installation, and maintenance," says Ee Huei Sin, vice president and general manager of Agilent's Basic Instruments Division. "This series also reaffirms our commitment to equip customers with not only the essential features of a handheld DMM, but also extra capabilities that help them do more quick checks in a wider range of situations."

The series comprises models U1241A and U1242A, which provide a range of measurement functions, including voltage, capacitance, and temperature. Key features include 10,000-count resolution, dual displays, a dual-intensity backlight, harmonic ratio, a switch counter, and data logging. The units also measure resistance to 100 MΩ and currents as small as 100 nA. Prices start at $200.

—by Dan Strassberg

▷**Agilent Technologies**, www.agilent.com/find/U1240A_pr.

The U1240A Series DMMs, whose features include dual displays and a dual-intensity backlight, can operate from either standard alkaline batteries or rechargeable batteries. Some of the manufacturer's handheld units even allow you to recharge the batteries while they remain inside the instrument.

10.11.07

SMART, SMALL FAN CONTROLLERS AND TEMPERATURE MONITORS SUPPORT PCs, EMBEDDED SYSTEMS

As power density increases in workstations and embedded systems, system controllers require more sophisticated temperature-control and device-monitoring capabilities. Addressing those needs, SMSC has introduced the EMC1046/47 and EMC1428 SMBus-temperature monitors and the EMC2103/4/5/6 family of fan controllers. Both product families incorporate the company's three proprietary high-accuracy measurement techniques–automatic beta compensation, antiparallel-diode technology, and resistance-error correction–to ensure 1°C accuracy.

Traditional temperature sensors require transistors with a flat gain, or "beta." However, at 45-nm geometry, transistor beta varies nonlinearly with the transistor's collector current, thus varying temperature accuracy. SMSC's automatic-beta-compensation method relies on measuring high and low collector currents it injects into the measurement transistor. This method meets transistor-model-measurement standards that Intel (www.intel.com) requires for its systems based on 45-nm and smaller technologies. The second technique, antiparallel-diode technology, allows you to measure multiple remote diodes with just two pins. The third technique addresses the fact that substrate diodes and board traces add series resistance. SMSC's resistance-error-correction technology compensates for this resistance without the need for measuring the traces and calculating compensation.

In addition to these techniques, the EMC2103/4/5/6 family of fan controllers uses closed-loop-rpm fan control with look-up tables to offload fan control from the system controller. Measuring the fan speed within a closed loop allows you to meet fan-control setpoints with 5% or better accuracy and maintain those setpoints over the life of the product. This feature is essential because an aging fan changes its response to a given drive signal over time. The EMC2105 and EMC2106 incorporate linear fan drivers that integrate the FET from the system and can drive as much as 600 mA. The EMC2103 and EMC2105 target use in one-fan systems, and the EMC2104 and EMC2106 can drive two fans by applying a second PWM (pulse-width-modulation) signal. An EEPROM can configure these fan controllers for systems without a host controller.

The EMC210x family ranges in price from $1.20 to $1.80 each, and SMBus-temperature sensors range in price from $1 to $1.40 (10,000) each.—by Margery Conner

▶**SMSC, www.smsc.com.**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Handheld, 50,000-count, true-rms DMMs capture trends, offer built-in help displays, other advanced features

Fluke Corp, a leading supplier of handheld electronic test-and-measurement instruments, has announced two 50,000-count, true-rms, logging multimeters that feature TrendCapture: the $499.95 model 287 for electronics professionals and the $529.95 model 289 for industrial applications. Both units feature 3.5-in., 320×240-pixel graphical displays with switchable white backlighting. Both also feature a logging function with expanded memory that stores as many as 10,000 readings for unattended monitoring of signals over time. Using the built-in TrendCapture capability, you can save multiple logging sessions and review the logged readings in graphical format directly on the meter display before you download the data to a PC.

For accurate measurement of complex signals, both the 287 and 289 make 100-kHz-bandwidth, true-rms voltage and current measurements. For ease of use, the units include built-in context-sensitive help screens; multiple save options; and automatic time stamping, which facilitates convenient recall of measurements. The 287 exhibits 0.025% maximum basic-dc error and includes a temperature-measurement function. Both units provide a 50,000-μF-capacitance range, offer peak capture to record transients as brief as 250 μsec, and can measure currents as great as 10A (20A for 30 sec). Both units also provide a relative mode that removes test-lead resistance from low-resistance and capacitance measurements.

The 289 has a two-terminal, 50Ω range with 1-mΩ resolution and 10-mA source current. This range is useful for measuring and comparing differences in motor-winding- and contact resistance. The 289 features a lowpass filter for accurate voltage and frequency measurements on adjustable-speed motor drives and other electrically noisy equipment. It also features a low-impedance voltage function that eliminates ghost voltages and facilitates testing for the presence of live circuits. The meter, which complies with second-edition IEC (International Electrotechnical Commission) and ANSI (American National Standards Institute) electrical-safety standards, withstands the 8000V spikes that load switching and industrial-circuit faults cause.

—by Dan Strassberg

▷**Fluke Corp,** www.fluke.com.

A 320×240-pixel backlit LCD enables the model 289 to simultaneously and clearly display the most recent measurement as well as the maximum, minimum, and average values of a series of measurements.

Nanotech supercapacitors up voltage, operating temperature

Supercapacitors combine the energy-storage capability of batteries with the rapid charge and discharge times of capacitors. They are good matches for applications with periodic pulsed loads that draw greater power than a battery can provide, such as LED flashes, autofocus motor drives for cameras, and cell-phone audio. Cap-xx has introduced the high-temperature HS and HW lines of supercapacitors that bump up the operating voltage from 4.5 to 5.5V and extend the operating and storage temperature from 75 to 85°C. Tolerance of high temperatures is important in supercapacitors for consumer electronics, such as those in vehicles sitting in direct sunlight or next to a heat-producing component, such as an RF power amp. Power densities are as high as 71.5 kW/l, and energy densities are as high as 1.5 Whr/l.

The HW series has a footprint of 28.5×17 mm, a height of 0.9 to 2.90 mm, capacitance as great as 0.4F at 5.5V, and ESR (equivalent-series resistance) as low as 110 mΩ at 5.5V. The HS series has a footprint of 39×17 mm, capacitance as great as 0.7F, and an ESR as low as 55 mΩ at 5.5V.

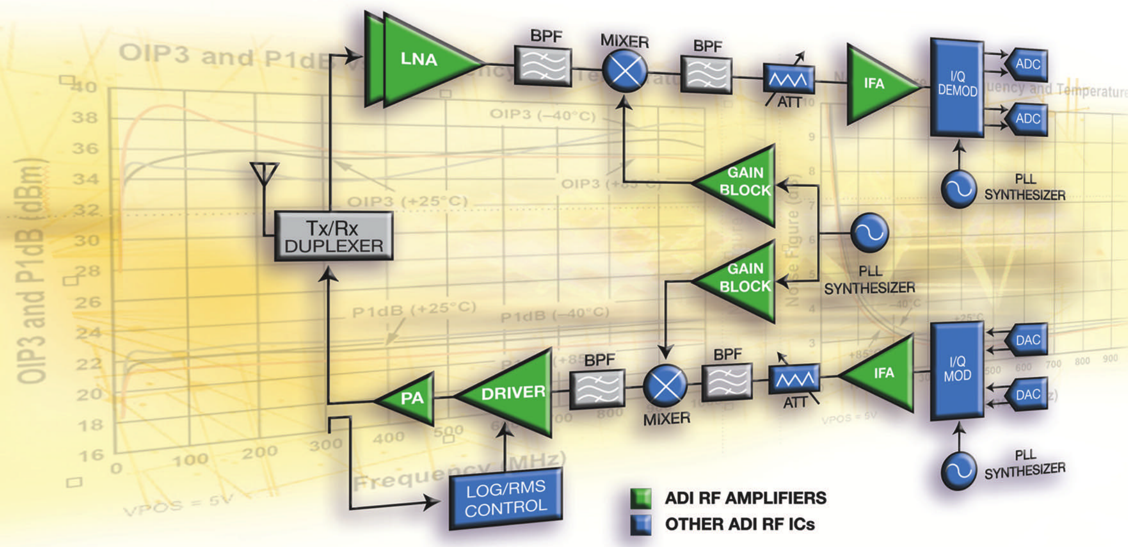
You can solder or ultrasonically weld the low-profile, prismatic packages to pads on a PCB (printed-circuit board). Pulse current for a single pulse is 20A; rms current is 4A. Prices start at less than $2 each (production quantities).

—by Margery Conner

▷**Cap-xx**, www.cap-xx.com.

Cap-xx's new HS and HW lines of supercapacitors feature an operating-temperature range of −40 to +85°C and an operating voltage of 5.5V.

The highest performance RF amplifiers. Across the signal chain, analog is everywhere.



Low Noise Amplifiers (LNA)

Part Number	Freq Range (MHz)	Gain (dB)	OIP3 (dBm)	P1dB (dBm)	NF (dB)	Current (mA)	Specs @ (MHz)	Price
ADL5521	400 to 4000	15.3	35.3	22.5	0.8	65	1950	$2.15
ADL5523	400 to 4000	17.5	33.7	21.9	1.0	65	1950	$2.15

Intermediate Frequency Amplifiers (IFA)

Part Number	Freq Range (MHz)	Gain (dB)	OIP3 (dBm)	P1dB (dBm)	NF (dB)	Current (mA)	Specs @ (MHz)	Price
ADL5530*	DC to 1000	16.8	37.0	21.8	3.0	110	190	$1.56
ADL5531	20 to 500	20.3	40.9	20.7	2.7	101	190	$2.25
ADL5532	20 to 500	16.1	39.1	19.7	3.0	95	70	$2.25
ADL5533 (75 Ω)	30 to 1000	19.8	37.3	18.7	2.9	66	70	$2.55
ADL5534 (Dual)	20 to 500	19.8	41.8	20.0	2.5	90	70	$3.29

Gain Blocks

Part Number	Freq Range (MHz)	Gain (dB)	OIP3 (dBm)	P1dB (dBm)	NF (dB)	Current (mA)	Specs @ (MHz)	Price
AD8353*	1 to 2700	19.5	22.8	8.3	5.6	42	900	$0.48
AD8354*	1 to 2700	19.5	19.3	4.8	4.4	25	900	$0.48
ADL5541	50 to 6000	14.7	39.2	16.3	3.8	92	2000	$1.65
ADL5542	50 to 6000	18.7	39.0	18.0	3.2	92	2000	$1.65

Driver Amplifiers

Part Number	Freq Range (MHz)	Gain (dB)	OIP3 (dBm)	P1dB (dBm)	NF (dB)	Current (mA)	Specs @ (MHz)	Price
ADL5320	400 to 2700	13.7	42.0	25.6	4.2	104	2140	$2.55
ADL5322	700 to 1000	19.9	45.3	27.9	5.0	320	900	$3.48
ADL5323	1700 to 2400	19.5	43.5	28.0	5.0	320	2140	$3.48

*3 V bias is also supported.
All prices shown are $U.S. in 1k quantities unless otherwise noted.

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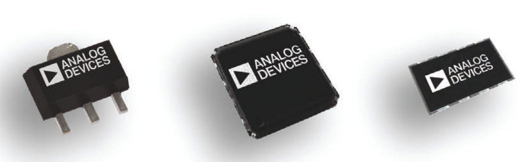

RF amplifiers available in 8-lead LFCSP, 16-lead LFCSP, and SOT-89 packages—from 6 mm² to 16 mm²—with single/dual options

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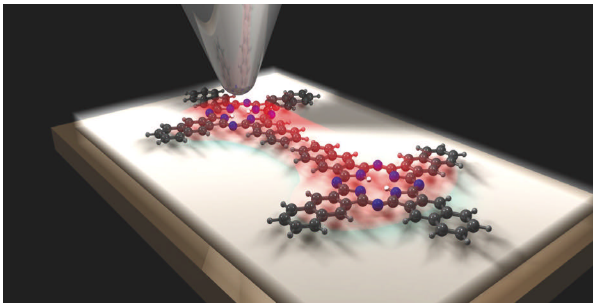


In an IBM-developed process, a tunneling-microscope probe impels hydrogen atoms within an organic molecule to switch places, thus switching from logic one to logic zero or vice versa.

RESEARCH UPDATE

BY MATTHEW MILLER

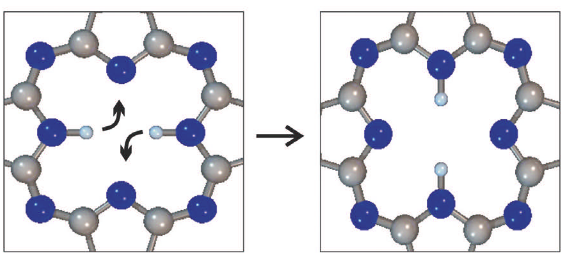
IBM claims single-molecule logic switching

Researchers at IBM have demonstrated logic switching among single molecules in a stable structure that better suits circuit construction than earlier molecular switches. The technique employs the probe of a low-temperature, scanning, tunneling microscope to induce a voltage pulse in a molecule of naphthalocyanine. The voltage pulse impels two hydrogen atoms within the molecule to change position, thus turning the switch on or off.

Research teams at IBM and elsewhere have previously demonstrated molecular switches. But those devices employed complex 3-D molecules that changed their shape when switching, making them ill-suited to serve as circuit-building blocks, according to the researchers. The molecular "frame" in the IBM technique, by contrast, maintains its shape and stability, which should make it easier to arrange the molecules on a surface and couple them in a controlled way. For its next trick, the research team plans to build a series of such molecules into a circuit and then move on to networking such circuits together into molecular chips.

As often happens in science, the discovery emerged at least partially by accident, thereby underscoring the need for ongoing basic research. The researchers started working with naphthalocyanine to study molecular vibrations in general. When they noticed with surprise that the molecule's properties made it intriguing as a molecular switch, they shifted the focus of their work.

▷**IBM Research**, www.research.ibm.com.



A schematic view of the organic molecule before (left) and after switching (right) shows how the positions of the two hydrogen atoms change while the rest of the molecular frame remains unperturbed.

Size matters, even in nanometers

NIST (National Institute of Standards and Technology) has reported that the length of SWCNTs (single-walled carbon nanotubes) has a significant impact on their optical properties, including absorption, near-infrared fluorescence, and resonance Raman scattering. (In this phenomenon, when light passes through a transparent sample, a fraction of the light scatters in all directions. Most of the scattered photons are of the same wavelength of the incident light. However, in Raman scattering, a small fraction of the scattered light has a different wavelength.) Researchers typically consider such properties to be constants when working with materials at conventional scales, but NIST's close examination of 50- to 500-nm-long nanotubes revealed length-driven variability that may arise from quantum physical effects. That variability could prove useful when it comes to building SWCNTs into applications such as tiny optical sensors and biological probes, according to the scientists.

▷**National Institute of Standards and Technology**, www.nist.gov.

THERMOCHEMICAL PROCESS YIELDS NANOSCALE LITHOGRAPHY

Researchers at the Georgia Institute of Technology have developed what they claim is a fast, reliable, environmentally flexible, commercially viable way of creating nanoscale structures. The technique, TCNL (thermochemical nanolithography), employs the heated tip of an atomic-force microscope to induce a chemical reaction on the surface of a thin polymer film. The reaction changes the film from a hydrophobic to a hydrophilic substance—enabling the researchers to subsequently attach materials such as metal ions to the heat-exposed regions.

The method can write at speeds of millimeters per second, orders of magnitude faster than the 0.0001 mm/sec of dip-pen lithography, in which a microscope probe deposits its material on a surface. Moreover, TCNL can function outside a vacuum and should scale easily using arrays of atomic-force-microscope tips.

To see TCNL in action, go to www.edn.com/071011ru1.

▶Georgia Institute of Technology, www.gatech.edu.

The Georgia Institute of Technology researchers show their school spirit by using thermochemical nanolithography to write on a polymer film.

10.11.07

BY GARY GIUST, PHD

Setting up your oscilloscope to measure jitter

Half the battle in measuring jitter is simply setting up the oscilloscope. The goal here is to capture and display the signal as it would appear in its system environment. Because real-time oscilloscopes are workhorses in any laboratory, it's important to know how to get the most out of them. Jitter measurements are particularly sensitive to their environment. Consider some ways of optimizing this environment for measuring all types of jitter.

Begin by selecting an instrument with a proper bandwidth. If the bandwidth is too low, measured edge rates appear slow. Slower edge rates more efficiently convert amplitude noise into timing errors. An excessively high bandwidth, however, only raises the noise floor by increasing the thermal and shot noise in the measurement. A bandwidth of 1.8 times the bit rate is a good rule of thumb for NRZ (non-return-to-zero) data.

Next, set the sampling rate high enough to avoid aliasing effects from undersampling. In theory, the sampling rate must be at least twice the highest fundamental frequency in the signal. In practice, analog-signal-conditioning and data-conversion processes inherent in the acquisition use additional bandwidth, such that oscilloscopes realistically need a minimum sampling rate of 2.5 to three times this frequency. Oscilloscope manufacturers therefore ship instruments with bandwidth-to-sampling-rate ratios of approximately 1-to-3.

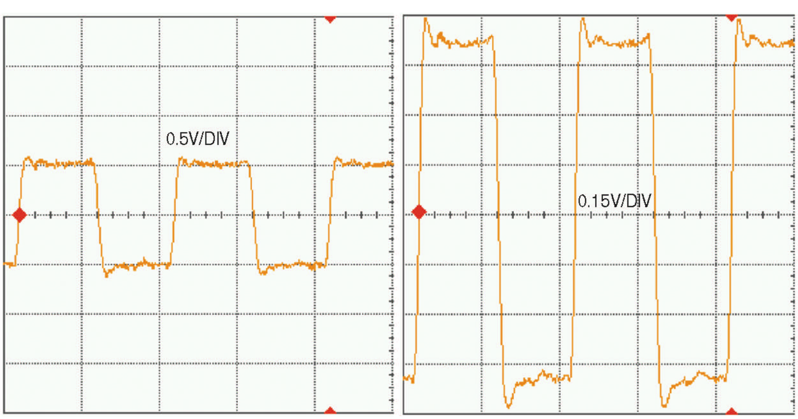
Maximizing the instrument's vertical resolution is critical for minimizing ADC quantization error. Adjust the volts-per-division knob until the image just fills the vertical height of the display. Overfilling the display saturates the ADC converter, whereas underfilling it reduces SNR (signal-to-noise ratio). **Figure 1** shows how this simple adjustment can dramatically improve measurement results.

The timebase setting is also important to consider when measuring TIE (time-interval-error) jitter, because this setting acts as an adjustable high-pass jitter filter. The timebase sets the lowest TIE frequency that the measurement captures. (The oscilloscope's bandwidth sets the highest jitter frequency.)

Also, make sure to test with data patterns containing a suitable range of frequency content. And, test using data patterns with realistic frequency content. When using PRBS (pseudo-random-bit-sequence) patterns, use pattern lengths long enough to capture low-frequency effects but short enough for the instrument's memory depth to fully capture them.

Always minimize the delay between the trigger and first sampled data point. After the signal is triggered, the timing uncertainty is proportional to how long the timebase waits before sampling the data. Reducing this delay minimizes this timing uncertainty, thereby lowering the measured jitter value.

Avoid oscilloscope modes that average the waveform, select sin(x)/x interpolation between data points, and use fast triggers with large amplitudes. Finally, set the trigger voltage to agree with the real system's receiver threshold voltage if you know it; otherwise, set it to the waveform's 50% level. **EDN**

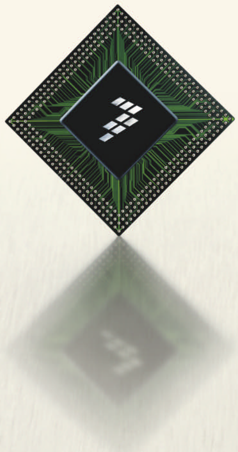


Jitter	0.5V/div	0.15V/div	Reduction (%)
Time-interval error	59	39	34
Period jitter	75	41	45
Cycle-to-cycle jitter	137	72	48

Note: Measure jitter in peak-to-peak picoseconds.

Figure 1 Changing the vertical resolution for this 100-MHz 1V p-p signal from 0.5V/division (left) to 0.15V/division (right) dramatically improves the measured jitter by reducing ADC quantization errors.

Gary Giust, PhD, is a marketing manager at PhaseLink Corp. He also conducts seminars through JitterTime Consulting. Contact him at garyg@phaselink.com.



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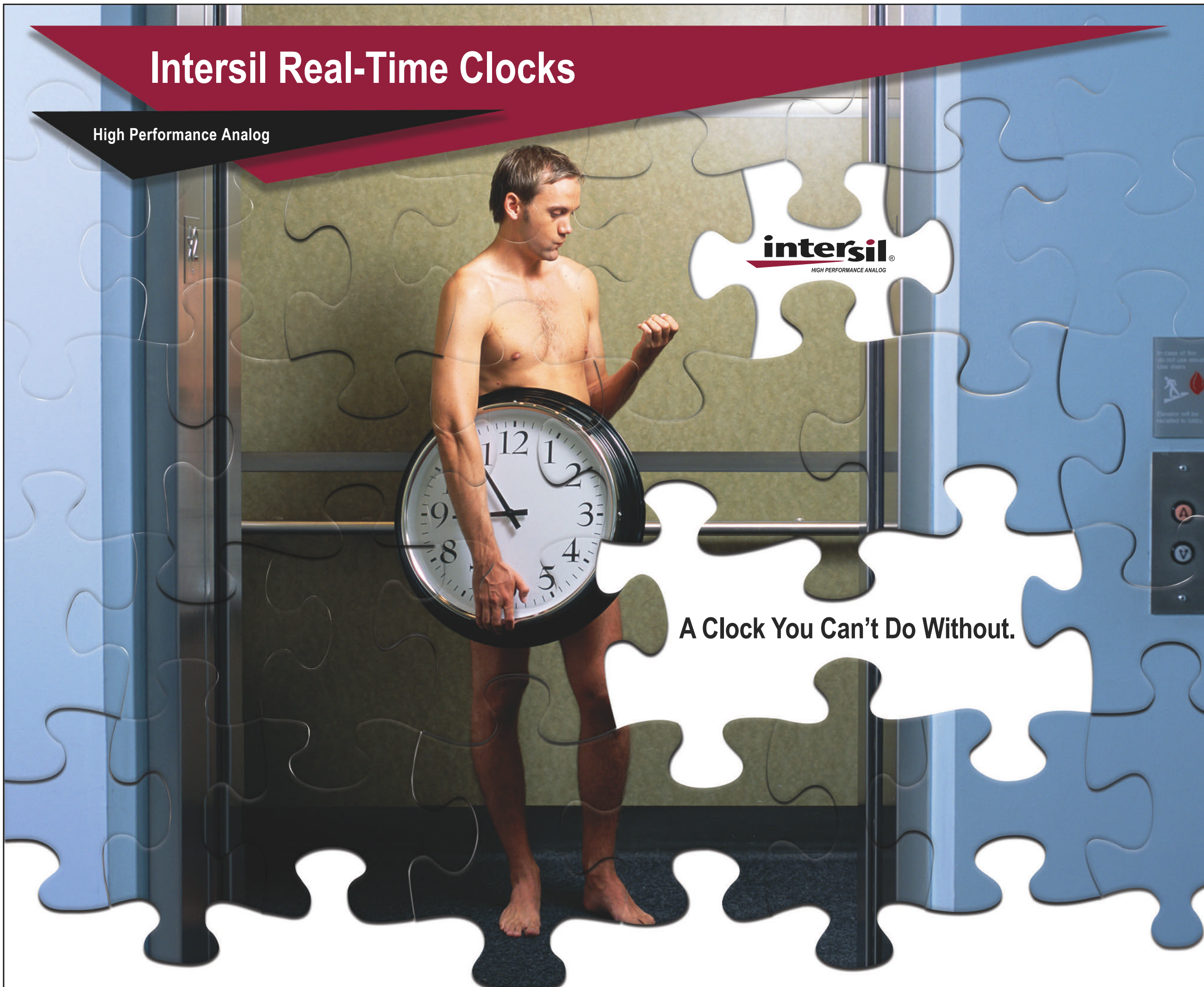

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4G wireless: EVOLUTION OR WATERSHED IN SOC ARCHITECTURES?

BY RON WILSON • EXECUTIVE EDITOR

The almost-mythological fourth generation of wireless service—4G—could be the fountainhead of an entirely new way of thinking about SOC (system-on-chip) architectures. Or it could drive a simple evolution of today's baseband wireless ICs. It could lead to entirely new kinds of mobile services for consumer clients. Or it could simply handle your e-mail attachments better. It could be a massive engineering challenge struggling into reality in 2015. Or it could happen in a couple of years.

To understand the impact that 4G is likely to have upon SOC design, you have to dig a little bit into just what people mean by the term, understand some of the computing challenges involved in supporting the service, and hear from some system architects on how they are approaching these challenges.

Many of the differences of opinion about the impact of 4G come from a single source: the lack of a clear definition. "You have to start with definitions," warns Bill Krenik, Texas Instruments' chief technology officer for wireless, "because all the controversy and confusion surrounding the term have left it meaning very little."

Many people, Krenik says, think of 4G in terms of a new world of ubiquitous wireless connectivity—really anywhere, all the time—and in terms of the interactive, location-based, and media-rich services that such connectivity can support. Imagine walking down the street in an unfamiliar town, holding up your handset, and seeing it continuously display a real-time moving image of the street in front of you with map data, labels on buildings and sites of interest, paths to possible destinations, and locations of persons in your address file as you walk. Or imagine that same handset turning the streets of the town into a multiplayer video game, complete with avatars for other players, 3-D images of aliens and weapons, and realistic rendering of the damage resulting from the virtual battle.

Others—who have to implement the underlying systems—often see 4G in more concrete terms. "Within TI, we don't try to have a dogmatic definition of what 4G is," Krenik explains. "Instead, we refer to the actual technologies by name: HSPA+ [high-speed packet access plus], WiMax, LTE [long-term evolution]. Until 3G Americas comes up with a standard, everything else is just opinion," he continues, referring to an organization whose mission is to promote the deployment of GSM (Global System for Mobile) communications and its evolution to 3G.

Still other engineers take a more quantitative view. Paralleling 3GPP's (Third Generation Partnership Project's) approach in defining LTE, these engineers frame 4G as "100-Mbps-peak throughput for mobile devices and 1-

Gbps peak for nomadic devices such as notebook computers," says Alan Brown, a senior radio-product manager at Nokia Siemens Networks. Each of these perspectives leads to a different set of expectations for the baseband SOC that will implement the 4G handset.

EVOLVING A BASEBAND SOC

Start with the simplest set of expectations—those that LTE envisions—that the mobile device will somehow achieve a downlink peak data rate of at least 100 Mbps. "This [situation] leads to a baseband that is functionally no different from what we use today for UMTS [Universal Mobile Telecommunications System]," says Freescale Semiconductor Vice President and Senior Fellow Ken Hansen. Blocks include hardware accelerators for sample-rate functions, a CPU core to execute the MAC (media-access controller), a security engine, and a host interface.

At sample rate, data coming from the radio goes through analog-to-digital conversion, through some front-end digital processing, and into an FFT (fast-Fourier-transform) engine that separates the OFDM (orthogonal-frequency-division-multiplexed) signal into its many constituent frequency bands. The frequency-domain signal then goes through further digital conditioning and into a detector—not unlike the read channel in a disk drive—that decodes the 64 QAM (quadrature-amplitude-modulation) signal on each of the carriers, producing a symbol from each active carrier. The symbols go through turbo decoding for decompression.

> **AT A GLANCE**
>
> - Fourth-generation wireless service, or 4G, means different things to different people.
> - Designers can achieve halfway measures with current chip architectures.
> - Cost and energy constraints will eventually force some architectural innovation.
> - The 4G that application developers dream of may require the use of radical architectures.

The difference between 3G and 4G in this architecture is a difference of quantity, not kind. "In 3G, we extract about 1 bps per hertz of bandwidth," points out Peter Carson, senior director of product management at Qualcomm CDMA Technologies. "To achieve 100-Mbps throughput, a 4G baseband would have to do significantly better than that: at least 3 or 4 bps per hertz, over a much wider band."

In practice, this situation means many more carrier frequencies spread over a 20-MHz channel, compared, for instance, with the 5-MHz channel that UMTS 900 uses. It may also mean using multiple antennas in a MIMO (multiple-input/multiple-output) configuration. Today, MIMO configurations most often see use in channel equalization: You find a way to combine the signals from the two antennas to get the best possible reception. But 4G has something else in mind: using beam-forming algorithms to in effect make each pair of a base-station antenna and a receiver antenna into a separate channel, thus multiplying the effective bandwidth. "With multiple receivers, research has demonstrated, you can get about 1.75 times the data rate with two antennas," Hansen says.

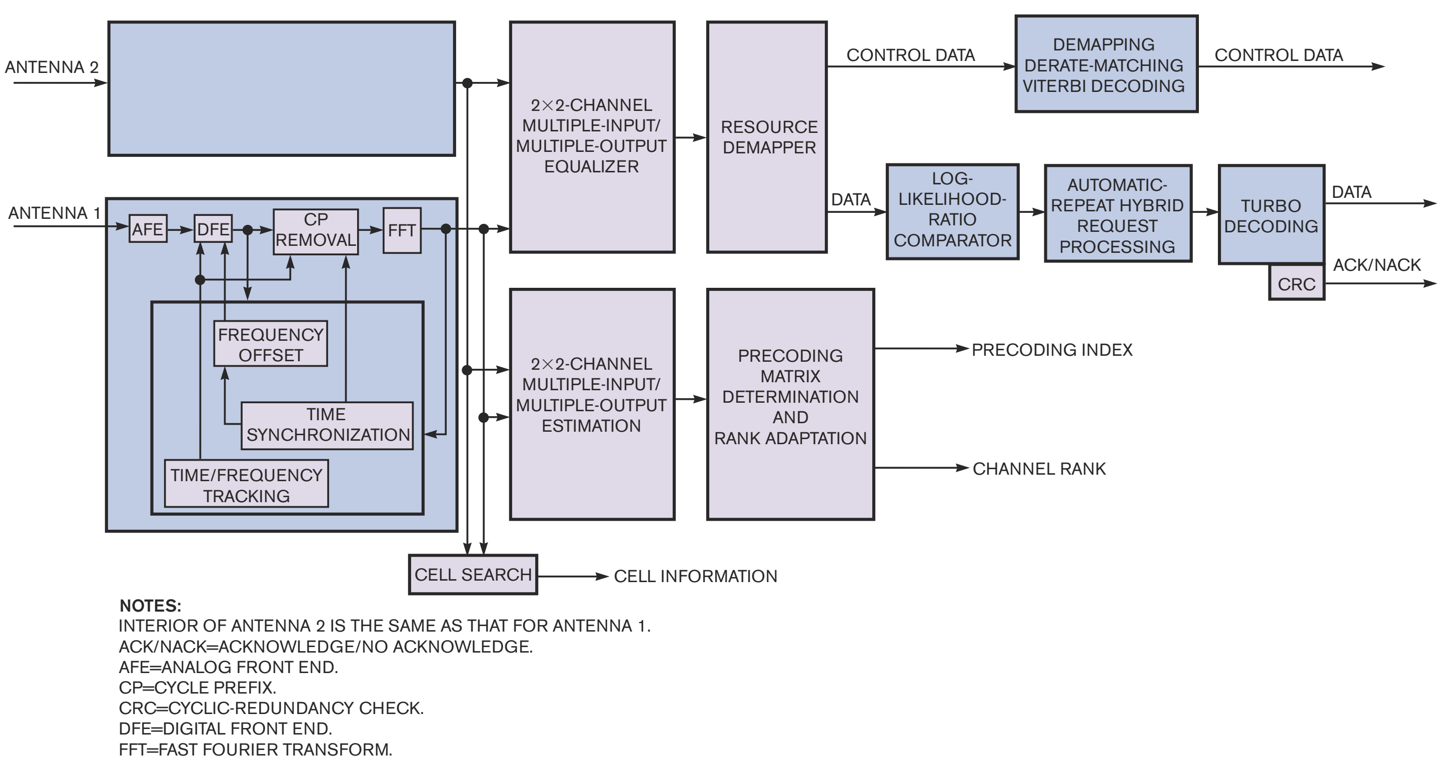

Figure 1 Infineon's vision of a downlink receiver for LTE shows the complexity of dealing with even two-antenna MIMO.

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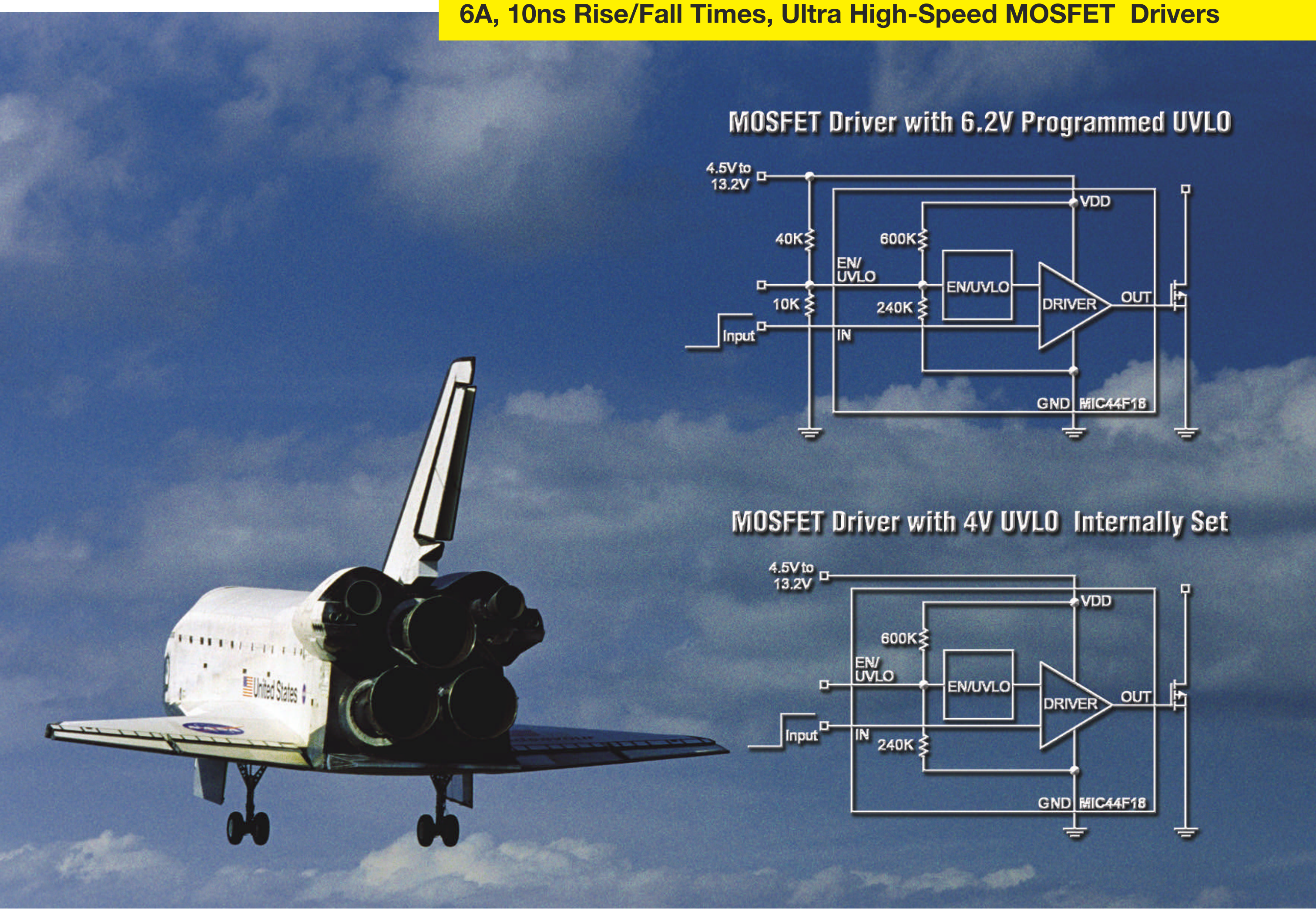

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All of this capability requires silicon. The higher sample rate and wider channel mean a bigger, more power-hungry ADC and a faster, wider FFT engine. But the big hit comes from the need to provide for a 100-Mbps-peak throughput, which means faster symbol-rate processors, a lot more memory, and a faster processor for the MAC. "We are looking at 10 times the data rate coming into the MAC, with one-tenth the allowable latency on some transactions," Hansen says. "But for power reasons, the MAC hardware has to run at a frequency much lower than the bit rate. This [problem] is interesting."

Qualcomm's Carson agrees. "Peak data rate turns directly into die size. One thing architects will have to ask themselves is whether the specified peak data rate and the die size it requires will be justified in the average data rate the network will actually deliver."

Given sufficient insensitivity to chip cost, the baseband architecture for this rate can be evolutionary. Carson says that Qualcomm's current Snapdragon architecture is still perfectly manageable extended to 30- to 40-Mbps-peak data rates. That speed doesn't meet the LTE specification, but LTE will come later—some call it late-term evolution—possibly allowing time for 32-nm CMOS to once again bail out the architects.

NONEVOLUTIONARY DESIGN

One of the first challenges to evolutionary architecture will come from MIMO. "MIMO is used to improve the quality of the wireless link," explains Thuyen Le, PhD, of the Feature Phone Business Unit, Communication Business Group of Infineon Technologies AG. "One idea is to use it for transmitter and receiver diversity to combat fading. The other idea is to exploit fading for spatial multiplexing, which then allows transmitting independent data streams over the multiple transmitting antennas at the same time, hence increasing the user data rate. That [idea], however, depends on how well-conditioned the channel matrix is. So, my take is that MIMO is necessary to achieve high data rates, in light of both ideas."

When air-interface designers shift from using a pair of receiving antennas to improve channel equalization to actually creating multiple channels through spatial-division multiplexing, the amount of duplicate hardware in the radio rises dramatically. Each antenna needs its own analog front end and digital front end, and the radio also needs either replication or increased throughput for much of the digital baseband (**Figure 1**). This requirement in itself does not mandate architectural innovation—just more of the same—but then there is the matter of power.

A limiting factor in any 4G architecture is that the radio must handle 10 times the peak data rate at a fraction of current energy consumption to make room for the dramatic increase in application-level processing energy. Will Strauss, president of research company Forward Concepts, estimates that a 4G handset will eventually require 100 times the computing power of a current 3G offering. "Everyone's great hope is 32-nm processes," Strauss observes, "but the reality is that energy consumption isn't going down that much with new processes. What you gain in dynamic power you give back in leakage power. It may come down to finding novel architectures and power-management schemes or carrying a battery on your back for the handset."

Another factor drives consideration of novel architectures, as well. It is the previously mentioned disparity between simply stating a peak data rate, as the LTE specification does, and envisioning a new manner of using mobile devices, as do many of the visionaries who are evangelizing 4G to investors.

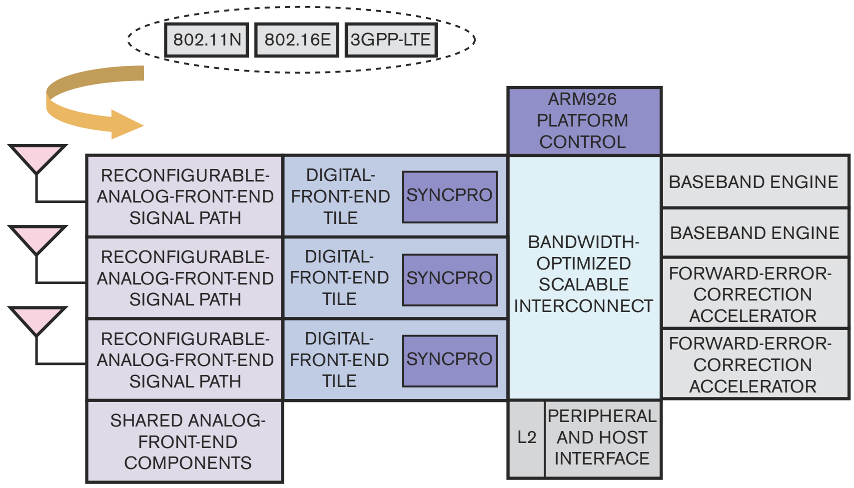

Figure 2 IMEC researchers envision an array of on-the-fly reconfigurable resources shifting instantly between air interfaces and channel conditions as bandwidth needs change.

IMAGINING THE FUTURE

"It's true there is no clear definition of 4G," says Liesbet Van der Perre, science director at IMEC (Interuniversity Microelectronics Center). "But I believe we should be talking of a heterogeneous network supporting much higher mobility and data rates than are currently possible. Today, if you are truly mobile, you will see less than 2 Mbps, but 4G should mean 10 to 20 Mbps of real throughput. At least 10 Mbits sustained—not peak—is essential for good video, for instance. One of the disappointments of 3G is that it could not deliver the sustained data rate for good video."

Van der Perre and other researchers describe an environment far more dynamic than anything that today's wireless networks can realize. "Today, a handset-silicon vendor faces something like 30 air interfaces, multiple noncontiguous channels, and many very dif-

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ferent services running simultaneously," she observes. But the fact that one phone from one vendor supports only a small subset of this cacophony simplifies much of this complexity.

In the future, to ensure both sufficient sustained bandwidth—think of that real-time video aligned to the moving handset's location and orientation—and sufficient energy efficiency—always choosing only just enough bandwidth and coding strength for the current task mix—a mobile device may be in continuous negotiation with a number of vendors, using a number of air interfaces from a number of base-station sites all at once (**Figure 2**). Bursts of data, video streams, control information, and a return channel from the keyboard and camera may all be traveling over different services and may switch in real time. For instance, holding the camera still allows the motion compensation in H.264 to drastically reduce the bit rate necessary to link the camera to a game-server farm. This action thus allows the radio controller to select an air interface with a lower bit rate.

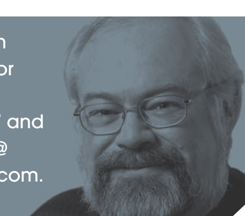
In this world view, using today's hardware-processing pipelines with dedicated blocks is an intermediate option, Van der Perre says. She sees modular, heterogeneous clusters of similar processors that you can specialize and a configurable interconnect network that can allow real-time dynamic processor configuration and task mapping. Aggressive energy-management techniques, including rapid voltage-frequency scaling, moderately fine-grained power-gating of idle units, and agile shifting of algorithms between software and hardware, become possible in such an architecture. Indeed, this approach may be the only way to meet the energy-efficiency demands of the true 4G terminal, 32-nm CMOS notwithstanding.

All of these elements are taking shape at IMEC in various research projects, which perhaps explains Van der Perre's world view. But it is far from an isolated point of view, at least in private. Companies publicly state their dedication to their pipeline-based hardware architectures, but one well-placed industry source claims that there are deeply embedded, heavily funded research teams at a number of major silicon suppliers exploring large multicore architectures for the 4G problem.

4G MAY BE THE FORGE ON WHICH DESIGNERS BEAT AN ENTIRELY NEW STYLE OF REAL-TIME EMBEDDED PROCESSING INTO SHAPE.

One major challenge with most large, multicore architectures is not an issue here: Much of the workload in high-bit-rate baseband processing is what the industry calls embarrassingly parallel. It's not hard to spread around the tasks by simply dividing up the data. But the system-control, dynamic-load-balancing, and—perhaps most important—energy-management tasks are new, complex, and vital to the success of the design. In this respect, 4G may in fact not be evolutionary but rather the forge on which designers beat an entirely new style of real-time embedded processing into shape. EDN

You can reach Executive Editor Ron Wilson at 1-408-345-4427 and ronald.wilson@reedbusiness.com.



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BY ROBERT CRAVOTTA • TECHNICAL EDITOR

Welcome to the 34th annual *EDN* microprocessor/microcontroller directory. Successful processor offerings for embedded-application designers stress the optimum balance of processing performance, power consumption, development resources, and bill-of-materials costs. The continuing, growing importance of this balance of application-specific features and software development is a focus of this year's directory. An obvious expansion of the online directory material is the inclusion of third-party-software-development companies.

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The number of companies and devices the directory lists continues to evolve, and we've added new entries to the company roster and to the table of devices and cores. The company roster and product listings continue to be testaments to the variety of processors available and the variation among requirements, features, and the types of applications for which designers are using microprocessors and microcontrollers. If you notice a company that we omitted, please let them and us know that you missed them and would like to see them in the next directory.

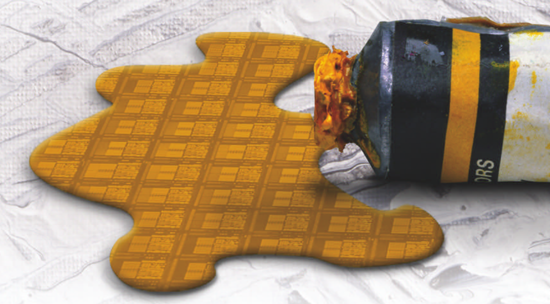
You can reach Technical Editor Robert Cravotta at 1-661-296-5096 and rcravotta@edn.com.

The print version of this directory is but a small fraction of the directory. Visiting the Web version at www.edn.com/microdirectory has taken on more importance as the company roster continues to expand the material well beyond the capacity of the print update. The print version lists the companies selling software-programmable processors and cores, provides an overview for each, and identifies the latest developments at each company.

This directory aims to provide designers and system architects enough visibility into processor options to quickly narrow the list of candidate processors for each project. The online version presents detailed information on each processor, including a specification table and block diagrams. The directory uses a common taxonomy for describing and categorizing target applications that helps you to quickly find and compare competing processors for your projects. The Web material has more details on the common application taxonomy.

The "Where are they?" **sidebar** on the Web helps you find companies that we no longer list, whether because they closed their doors, another company acquired them, or they spun off into another company. (Think NXP and Philips.)

If this directory helps you find or choose a device or core, please let the vendor know how you found its part. Help us continue to improve the directory by visiting us at www.edn.com/microdirectory or by sending your comments and feedback to microdirectory@edn.com.



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Actel offers the ARM Cortex-M1 and ARM7 processor cores for use in its optimized FPGA families without license fees or royalties. The FPGA-optimized, 32-bit Cortex-M1 processor core targets the company's flash-based ProASIC3 family, mixed-signal Actel Fusion PSCs (programmable-system chips), and low-power Igloo family. Actel also offers its CoreMP7, an optimized version of the ARM7 processor core, for its flash-based ProASIC3 FPGAs and Actel Fusion PSCs.

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Altium's Altium Designer development system combines board-level hardware, embedded software, and programmable hardware-development tools in a unified environment. It supports device- and vendor-independent electronic-product development using soft, hybrid, and discrete processors. It also supports interactive FPGA-system development. Altium Designer includes a number of royalty-free, 8- and 32-bit, FPGA-based soft processors, including Altium's FPGA-independent TSK3000RISC core. You can also use Altium Designer to target development for Nios II and MicroBlaze soft processors, the PowerPC within Xilinx's Virtex-II Pro devices, and discrete ARM7 and PowerPC devices.

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Analog Devices' ADuC7xxx precision analog microcontrollers combine embedded precision analog functions and digital programming in one chip that targets high-precision measurement-and-control and data-acquisition systems with basic digital-programming needs. The microcontrollers integrate a 32-bit RISC core and flash memory with precision data-conversion technology that supports as many as 16 channels of fast, 12-bit-accurate analog-to-digital conversion and as many as four 12-bit DACs.

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AMCC (Applied Micro Circuits Corp) offers embedded Power Architecture processors targeting control-plane, imaging, wireless-access, industrial-control, storage, and networking applications.

The company based the PowerPC 405EX on Power Architecture technology, and it targets 802.11n Wi-Fi- (wireless-fidelity) and WiMax-based wireless-access points and similar embedded-processing or network-control applications. AMCC also announced the PowerPC 460EX that targets high-performance applications, including multifunction printing, networking, and home gateways. AMCC and Intrinsity (www.intrinsity.com) joined forces to create a new Power Architecture processor core. Code-named Titan, the 32-bit semicustom core relies heavily on Intrinsity's Fast14 logic to reach clock speeds as high as 2 GHz in 90-nm bulk CMOS and consumes 2.5W. Titan is part of a dual-core "processor complex" that supports coherent multiprocessing.

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ARC also offers configurable, multistandard, preverified multimedia subsystems. ARC's newest subsystem, the ARC Video family, integrates a video-optimized, 32-bit ARC processor and as many as two ARC 128-bit SIMD (single-instruction/multiple-data) media engines, a media-optimized DMA engine, a multistandard entropy encoder and entropy decoder, a motion-estimation accelerator, and the VRaptor channel interconnect. ARC Sound and ARC Sound Advanced target audio-centric designs. ARC Player integrates voice, audio, and video-codec software with a media-optimized 32-bit ARC processor.

ARM, WWW.ARM.COM

ARM offers a range of processor cores, including the ARM7, ARM9, ARM10, and ARM11 families and the Cortex family featuring Thumb-2 technology. ARM also offers the SecurCore family targeting secure applications, such as smart cards and SIMs (subscriber-identity modules), the Mali family of graphics processors, and the OptimoDE (data-engine) signal-processing technology.

The high-performance ARM Cortex-A8 processor targets consumer products running multichannel video, audio, and gaming applications. For next-generation mobile devices, the ARM Cortex-A8 processor delivers performance with power consumption of less than 300 mW in a 65-nm technology. The midrange Cortex-R4 processor targets the performance requirements of next-generation embedded products, including mobile phones, hard-disk drives, printers, and automotive controllers. It features an advanced microarchitecture that can issue dual instructions.

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Asix Electronics offers highly integrated 8051/80390-based embedded processors that target applications such as home appliances, factory/building automation, industrial equipment, security systems, remote-control/monitoring/management, and streaming-media applications. The company's AX110xx family of 8-bit networked microcontrollers integrates a high-speed, pipelined, 100-MIPS 8051 core with 512 kbytes of flash memory. The embedded Ethernet PHY (physical) layer supports HP Auto-MDIX (media-dependent-interface crossover).

ATMEL, WWW.ATMEL.COM

Atmel's microcontrollers and DSCs (digital-signal controllers) include the 8-bit AVR and 32-bit AVR32, ARM7, ARM9, and ARM11 cores. With less than 1 μA of static power, the picoPower AVRs use power-saving technology that provides multiyear battery life in lighting-control, security, keyless-entry, ZigBee, and other applications that spend most of their time in sleep mode. Atmel's newest AVR32 UC3 microcontrollers use 40 mA at 66 MHz and 40 μA in sleep mode. Dual-banked pipelined flash and SRAM in the core support true single-cycle execution of 16-bit compact and 32-bit instructions.

Atmel's customizable ARM7 and ARM9 microcontrollers employ a metal-programmable block that integrates logic functions into a low-cost, single-chip system targeting low- to medium-volume designs. CAP (Customizable Atmel Processor) devices offer a power-performance-price proposition over microcontroller-plus-discrete-component options.

BROADCOM, WWW.BROADCOM.COM

Broadcom provides a family of high-performance, low-power, integrated processors targeting data-networking and communications applications, as well as security, storage, 3G-wireless infrastructure, and high-density computing.

The Broadcom broadband CMP (chip-multiprocessing) systems integrate as many as four 64-bit MIPS processor cores onto a single die. CMP scales system performance by sharing the workload across multiple cores.

CAMBRIDGE CONSULTANTS, WWW.CAMBRIDGECONSULTANTS.COM

Cambridge Consultants' XAP3, XAP4, and XAP5 family of RISC-processor soft cores targets low-cost ASIC products with high code density, high performance, low power, and small dice. Target applications include medical technology, industrial and consumer products, automotive systems, transportation, and wireless communications. The company's mixed-signal and wireless-SOC (system-on-chip) systems support several wireless standards.

XAP processors feature protected operating-system modes with register sets for user, supervisor, and interrupt code to provide secure operation when applications misbehave. Designers can implement the 16-bit XAP4 using as few as 12,000 gates. The 18,000-gate, 16-bit XAP5 processor has a 24-bit address bus that can run programs as large as 16 Mbytes. The 32-bit XAP3 processor has 30,000 gates.

CAST, WWW.CAST-INC.COM

Cast offers IP (intellectual-property) cores for general-purpose 8-, 16-, and 32-bit processors. Configurable 8051 cores target embedded systems needing more performance than an 8051 can offer. They require as few as 7000 gates, perform at 0.6 Dhrystone MIPS/MHz, and use as little as 18 µW/MHz of power. A coprocessor architecture enables performance improvement for specific applications, and an ASP-DSP coprocessor is available.

CAVIUM NETWORKS, WWW.CAVIUM.COM

Cavium Networks offers security and single-core and multicore MIPS64-based processors targeting networking, wireless, storage, and control-plane applications in the broadband consumer, SOHO (small-office/home-office), SME (small-and-midsized-enterprise), enterprise, data-center, telecom, ATCA (Advanced Telecom Computing Architecture), AMC (Advanced Mezzanine Card), 3G/4G, and service-provider markets.

The Octeon MIPS64 processors integrate one to 16 MIPS64 cores with high-performance networking, multicore acceleration, memory controllers, and advanced hardware-acceleration coprocessors for TCP (Transmission Control Protocol), compression, decompression, regular expression, and security.

CIRRUS LOGIC, WWW.CIRRUS.COM

Cirrus Logic supplies high-precision analog, mixed-signal, and embedded processors for the audio and industrial markets. The company offers highly integrated ARM9- and ARM7-based embedded general-purpose processors targeting industrial and networked consumer applications.

The company's NineSeries of ARM9-based products includes the EP9301, EP9302, EP9307, EP9312, and flagship EP9315. The entry-level EP9301 integrates Ethernet and two USB 2.0 host ports, and the EP9302 adds Maverick-Crunch and MaverickKey to go along with increased processing power and memory. The EP9307 adds a graphics accelerator, touchscreen and keypad support, and three USB ports. The EP9312 includes support for high-quality audio and an integrated development environment.

CRADLE TECHNOLOGIES, WWW.CRADLE.COM

Cradle's CT3600 family of scalable MDSP (multicore-digital-signal-processing) processors integrates multiple general-purpose processors with multiple DSPs to improve processor efficiency for control code and computationally intensive media-processing algorithms. Targeting media-processing applications, particularly those involving complex, intelligent-video applications, the CT3600 family comprises two products containing eight to 16 DSPs on one chip. The largest version, with 16 DSPs and eight general-purpose processors, operates at 350 MHz, supports 16 channels of CIF (common-intermediate-format)-resolution Simple Profile MPEG-4 encoding, and can perform more than 22,000 16-bit MMACs (million multiply/accumulate) operations/sec, quadrupling the total performance over Cradle's previous-generation MDSP.

CYAN TECHNOLOGY, WWW.CYANTECHNOLOGY.COM

Cyan Technology's low-power, 16-bit, embedded-communications, flash-based eCOG1k microcontroller implements a 25-MHz RISC Harvard architecture that includes internal flash memory, RAM, and cache. The external-memory interface supports addressability of 32 Mbytes of external memory. Additional features include a smart-card interface, a 12-bit ADC, a temperature sensor, and a proprietary-port configuration device.

CYBERNETIC MICRO SYSTEMS, WWW.CONTROLCHIPS.COM

Cybernetic Micro Systems produces ASICs to interface to peripherals that would be difficult to control from a general-purpose computer. The 100-pin, 8-bit P-51 microcontroller either sits between the host computer and the peripheral device or becomes the peripheral device. With a dual-port RAM interface on the host side in a PC104/ISA (industry-standard-architecture) format, the P-51 looks like memory to the host, but it has the intelligence and capability of an 8051.

CYPRESS MICROSYSTEMS, WWW.CYPRESSMICRO.COM

Cypress' system-level PSOC (programmable-system-on-chip) mixed-signal array has configurable digital and analog peripherals, an 8-bit microcontroller, and three types of embedded memory. PSOC target applications include automotive, communications, computers and peripherals, consumer, industrial, and mobile/wireless. PSOC integrates as many as 12 analog and 16 digital configurable hardware blocks in one device. PSOC blocks can implement a variety of user-selectable hardware-peripheral functions that you configure through register settings. The analog blocks encompass an operational amplifier and include programmable multiplexing and feedback characteristics. Each digital block is an 8-bit-wide resource; therefore, creating an 8-bit PWM (pulse-width modulator) requires one digital PSOC block.

DIGI INTERNATIONAL, WWW.DIGI.COM

Digi International offers net-centric Net+ARM processor SOCs (systems on chips) based on ARM7 and ARM9 cores. The NS9360, NS9750, and NS9775 employ the ARM926EJ-S core. The NS9360 operates at 177 MHz and integrates 10/100-Mbps Ethernet, a USB interface, an LCD, IEEE 1284, and serial I/O. The NS9750 operates at 200 MHz and includes all of the NS9360 features, plus PCI support. The high-performance NS9775 color-laser-printer processor operates at 200 MHz and integrates 10/100-Mbps Ethernet, a USB interface, and PCI to improve the cost performance of color laser printers.

new

DIGITAL CORE DESIGN, WWW.DCD.PL

DCD (Digital Core Design) provides VHDL and Verilog synthesizable, ISO 9001:2000-certified IP (intellectual-property) cores of 8-, 16-, and 32-bit processors and bus interfaces, as well as fixed- and floating-point arithmetic coprocessors. DCD's DP8051XP/DP80390XP soft core is 100% binary-compatible with the industry-standard 8051 8-bit microcontroller. Its SXDM (synchronous-external-data-memory) interface enables fast access to external data memory. DP8051XP/DP80390XP dual data pointers with automatic-increment, -decrement, and -switching capabilities significantly increase the speed of memory operations.

DCD's microcontrollers implement fast 16- and 32-bit integer operations and single- and double-precision floating-point operations. The new D68HC11 is fully compatible with the 68HC11A and 68HC11E.

EM MICROELECTRONIC, WWW.EMMICROELECTRONIC.COM

EM Microelectronic designs and produces ultralow-power, low-voltage, digital-, analog-, and mixed-signal ICs targeting battery-operated and field-powered devices in consumer, automotive, and industrial applications.

The company's 4- and 8-bit microcontrollers target battery-operated devices, which often have low-standby-power requirements and perform periodic or on-demand actions, such as fire alarms, medical monitoring devices, sports-activity monitors, radio-controlled clocks, intelligent sensors, data loggers, metering devices, intelligent terminals, card readers, and scales.

FREESCALE SEMICONDUCTOR, WWW.FREESCALE.COM

Freescale Semiconductor offers microcontrollers, embedded processors, sensors, RF components, analog/power-management technology, and supporting software for

automotive, consumer, industrial, networking, and wireless applications. The introduction of the Flexis QE 128 devices, targeting consumer and industrial applications, is part of Freescale's Controller Continuum road map, which provides pin-for-pin compatibility and a common set of on-chip peripherals and development tools for 8- and 32-bit microcontrollers. The company expanded its ColdFire portfolio with 10 new microcontrollers for low-power applications and 12 new high-performance microprocessors. The automotive line includes additions to controllers employing S08, S12X, and Power Architecture cores, as well as FlexRay-ready systems.

FUJITSU MICROELECTRONICS AMERICA, WWW.FMA.FUJITSU.COM

Fujitsu's 8-, 16-, and 32-bit microcontrollers include general-purpose and application-specific versions; most of the microcontrollers include onboard-flash, ROM, ADC, DAC, CAN (controller-area-network), USB, and LCD controllers to target automotive, communications, computer-peripheral, industrial, and consumer applications. A full complement of software- and hardware-development tools supports these microcontrollers. The F2MC (Fujitsu flexible-microcontroller) line includes the 8-bit F2MC-8L and F2MC-8FX series and the 16-bit F2MC-16L/16LX/16F series. The FR (Fujitsu RISC) series has a stepper motor and LCD controllers for auto, communications, computer-peripheral, industrial, consumer, and security applications.

new

GAINSPAN, WWW.GAINSPAN.COM

GainSpan is a Wi-Fi (wireless-fidelity) semiconductor and software provider for applications such as temperature monitoring for energy management, condition monitoring of industrial equipment, and street-light monitoring for metropolitan areas that require Wi-Fi capability and five to 10 years of battery life. The GainSpan GS1010 Wi-Fi SOC (system on chip) integrates an 802.11b/g radio, an ARM7 microcontroller, and a power-management unit. The GMS (GainSpan-management-system) software manages Wi-Fi devices that are asleep as much as possible to conserve energy. GMS resides in the network as an "always-on" intelligent interface.

HYPERSTONE, WWW.HYPERSTONE.COM

This year, Hyperstone introduced the low-cost E2 RISC/DSP that targets cost-sensitive audio and consumer applications by integrating an E1-32XSR RISC/DSP core, a high-speed serial-communication engine, 32 kbytes of SRAM, an SDRAM interface, and a multiplexed input.

Hyperstone's E1-16XSR/32XSR RISC/DSPs feature dual RISC and DSP execution units in a pipelined architecture sharing the same registers. Designers can transparently mix RISC- and DSP-specific programming. The RISC/DSP instructions execute with a high degree of parallelism. Target applications are telephony, VOIP (voice-over-Internet Protocol) telephony, video, digital cameras, and general signal processing.

Hyperstone built the HyNet32XS/32S series of networking processors around the E1-32XSR core. They target applications requiring high-speed signal processing and communications.

IBM, WWW.IBM.COM

IBM Global Engineering Solutions offers embedded microprocessor cores and microprocessors employing IBM Power Architecture technology. IBM's offerings include the 32-bit PowerPC 4xx family of embedded cores, along with 32- and 64-bit power- and performance-optimized microprocessors. The company's PowerPC 405, 440, and 460 families of embedded cores offer scalable performance for custom-SOC (system-on-chip) integration. The cores are available in both fab-optimized and fully synthesizable versions.

IBM's PowerPC 750 family of 32-bit microprocessors targets cost- and power-sensitive embedded-system applications. The newest addition to the 750 family, the 750CL, is available at speeds as high as 1 GHz. The PowerPC 970 family of microprocessors offers a performance-driven 64-bit architecture with native 32-bit application compatibility. Targeting computationally and bandwidth-intensive workloads, IBM's 970 family includes both single- and dual-core, VMX (virtual-machine-extensions)-enabled microprocessors.

new

IMEC, WWW.IMEC.BE

IMEC's (Interuniversity Microelectronic Center's) flexible ADRES (architecture for dynamically reconfigurable embedded system) consists of a tightly coupled VLIW (very-long-instruction-word) processor and a coarse-grained reconfigurable array.

The architecture template consists of computational, storage, and routing resources. The routing resources connect the computational and storage resources in a topology to form the ADRES array. Data accesses to the memory of the unified architecture take place through load/store operations. A script-based technique allows designers to generate instances by specifying different values for the communication topology, supported operation set, resource allocation, and timing of the target architecture.

IMSYS TECHNOLOGIES, WWW.IMSYSTECH.COM

Imsys develops reconfigurable-processor platforms that accept programs written in Java, C/C++, assembler, and microcode. The company offers Internet-enabled reference modules that Imsys ships as ready-to-go subsystems with complete operating- and file-system environments. The integrated hardware and software platform targets wired and wireless communications; graphics-display technologies; and image processing in telecom, automotive, industrial-automation, and consumer electronics.

INFINEON TECHNOLOGIES, WWW.INFINEON.COM

This year, Infineon introduced a 16-bit, industrial DSC (digital-signal-controller) family and extended its automotive portfolio with a high-performance, 16-bit microcontroller family; a cost-effective, 32-bit microcontroller for power trains; and an 8-bit series for high-temperature environments.

The XE166 DSC optimizes high-performance motor-control applications with an integrated MAC (multiply/accumulate) unit and supporting libraries and peripherals, including dual ADCs, user-configurable serial interfaces, and as many as 12 complementary pairs of PWM (pulse-width-modulation) I/Os for multiple motors. The XC2200 family of 16-bit microcontrollers fulfills all the key requirements for current and future automotive-body and gateway applications.

The TC1764 is the newest member of Infineon's family of 32-bit TriCore microcontrollers targeting automotive-electronics applications. The 8-bit XC866 Hot microcontrollers operate at temperatures as high as 140°C.

INTEGRATED DEVICE TECHNOLOGY, WWW.IDT.COM

The IDT Interprise family of integrated communications processors delivers data processing at line-rate speed. IDT based the processor cores on the 32-bit MIPS ISA (instruction-set architecture). Interprise processors target SOHO (small-office/home-office) routers, Ethernet switches, wireless-access points, and VPN (virtual-private-network) equipment.

INTEL, WWW.INTEL.COM

The Intel Core2 Duo E6400 and T7400 processors offer energy-efficient performance to help equipment manufacturers balance processing capabilities within power and space constraints. The processors target interactive computers, such as gaming platforms and industrial-control and -automation, digital-security-surveillance, medical-imaging, and communications applications.

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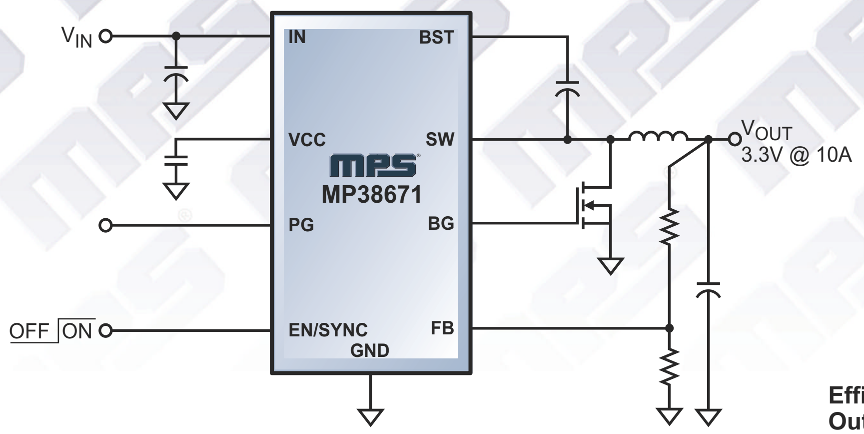

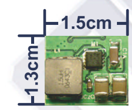

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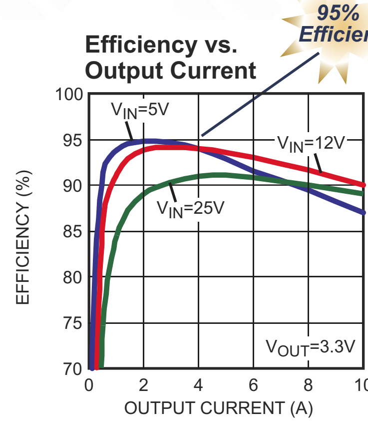

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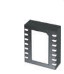
MP38891	420KHz	4.5 - 30	0.8 - 15	6	
MP38874	600KHz	4.5 - 21	0.8 - 15	8	
MP38671	600KHz	4.5 - 28	0.8 - 15	10	



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series is the first Intel-architecture-based quad core for the embedded-system segment. These processors target applications with computationally intensive and I/O-intensive workloads in high-end communications and enterprise systems.

INTELLASYS, WWW.INTELLASYS.NET

IntellaSys based its multicore chips on the proprietary SEA (Scalable Embedded Array) Platform, which uses a dual-stack, synchronous, scalable architecture. The inaugural SEAforth-24 family packs a 634-processor array of 18-bit processors, each of which can operate at 1 BOPS (billion operations per second). Designers can dedicate any of the 24 cores individually or in groups to perform tasks. Because each core has its own ROM and RAM, there is no need to use external memory for the bulk of processing and data accesses. The SEAforth-24 directly drives an antenna, eliminating the need for external data converters.

Communications between nearest neighbors takes place through dedicated registers that automate the process. A core waiting for data from a neighbor automatically goes to sleep, dissipating only a few microwatts.

IntellaSys expanded its offerings with the acquisition of Indigita secure-content processors and OnSpec secure-storage controllers. Indigita's products enable direct-to-disk HDTV (high-definition-television) dual-digital-stream recording at high data rates and provide multiple levels of security that preserve the Fair Usage rights of consumers and protect commercial interests.

IPFLEX, WWW.IPFLEX.COM/EN

IPFlex offers dynamically reconfigurable processors and design-tool platforms targeting industrial-image-processing, network-security, and scientific-computing applications. The DAPDNA (digital-application-processor/distributed-network-architecture) series of processors incorporate a RISC processor as a controller and a heterogeneous matrix of 300 to 1000 16- to 32-bit processing elements that the system can reconfigure in a single clock cycle. The DAPDNA-2 and DAPDNA-IMS processors target image-inspection-system, network-security, and multifunction-printer applications. The DAPDNA partner program includes 15 design-service partners in the United States and Japan.

The design-tool suite includes a Data Flow C compiler that IPFlex jointly developed with Celoxica (www.celoxica.com). The compiler enables designers to describe algorithms in a C-like syntax, which is partly based on Handel-C, and automatically generates hardware code.

KAWASAKI MICROELECTRONICS (K-MICRO), WWW.K-MICRO.US

K-Micro's ASIC technologies and design support target consumer-electronics, computer, office-automation, networking, and storage markets. K-Micro's computing subsystem includes a MIPS32 24Kf processor, the Sonics SiliconBackplane and Sonics3220 Smart interconnects, the SafeNet SafeXcel security engine, an off-chip OCP (Open Core Protocol) interface, on-chip SRAM, a flash-memory controller, a DMA interface, an interrupt controller, and a timer. To create an SOC (system on chip), designers add their proprietary logic to the computing subsystem. Single- and dual-core processors are available.

LATTICE SEMICONDUCTOR, WWW.LATTICESEMI.COM

The 32-bit LatticeMico32 open-source soft-microcontroller core combines a 32-bit-wide instruction set with 32 general-purpose registers. The architecture is configurable with a RISC-like instruction set. Based on the Wishbone bus of OpenCores, it employs independent instruction paths and datapaths.

The license preserves the open nature of the core by permitting use alongside proprietary designs and allows hardware implementation and distribution without the need for a subsequent license agreement. Lattice also provides the Mico System Builder for creating a LatticeMico32 system. The LatticeMico32 comes with GNU-based C/C++ software-development tools and an instruction-set simulator. Lattice provides an open-source 8-bit microcontroller and the 8051, PIC, and 6502.

LUMINARY MICRO, WWW.LUMINARYMICRO.COM

Luminary Micro designs, markets, and sells more than 80 ARM Cortex-M3-based microcontrollers. The Cortex-M3 processors provide 32-bit performance and integration for a price similar to that of 8- and 16-bit devices. The Stellaris family targets applications requiring control processing and connectivity, such as motion control, medical instrumentation, HVAC (heating/ventilation/air conditioning) and building control, factory automation, transportation, remote monitoring, electronic point-of-sales machines, network appliances, and gaming equipment.

Recently, the company released several Stellaris products featuring new combinations of industrial connectivity, expanded motion-control I/O, more on-chip memory, and low-power optimization for battery-backed applications. The newest Stellaris microcontrollers feature as much as 62.5 Dhrystone MIPS operation at 50 MHz and as much as 256 and 64 kbytes of single-cycle industrial-grade flash and SRAM, respectively.

MAXIM INTEGRATED PRODUCTS, WWW.MAXIM-IC.COM

Maxim Integrated Products offers networked, secure, mixed-signal, and 8051-drop-in families of microcontrollers. The network microcontrollers provide low-cost connections for networking applications and optionally include a complete TCP/IP (Transmission Control Protocol/Internet Protocol) network stack in ROM, a built-in Ethernet MAC (media-access controller), CAN (controller-area networking), and parallel and serial ports. The devices use a four-clock-per-machine-cycle 8051 core with an extended 22-bit addressing range and 16-Mbyte direct addressing.

The secure microcontrollers target applications demanding protective measures against theft of proprietary or secret information. These devices employ encryption and physical-protection techniques that support point-of-sale terminals, automated-teller machines, banking equipment, and gaming equipment.

MICROCHIP TECHNOLOGY, WWW.MICROCHIP.COM

Microchip offers 8- and 16-bit PIC microcontrollers, as well as 16-bit dsPIC DSCs (digital-signal controllers). The company based the 8-bit PIC microcontrollers on a RISC-core architecture that enables designers to migrate from six- to 100-pin devices among all families with little or no code changes. All of Microchip's 92 16-bit microcontroller and DSC devices are pinout-, software-, and peripheral-compatible with each other.

Microchip introduced several general-purpose 8- and 16-bit microcontrollers and developments tools. Highlights for 8-bit devices include the PIC18F97J60 with an onboard Ethernet controller, as well as the flash PIC16F616/HV616 families with peripherals to enable cost-effective fan or small-motor control. New 16-bit offerings include the PIC24FJ64GA00X family that supports a PPS (peripheral-pin-select) pin-mapping function. New high-performance devices include two PIC24H microcontrollers and four dsPIC33F DSCs for smart-sensor-processing applications, as well as a family of dsPIC33F DSCs targeting high-performance, sensorless motor-control applications with support for advanced motor-control algorithms, such as FOC (field-oriented control).

MIPS TECHNOLOGIES, WWW.MIPS.COM

MIPS Technologies licenses 32- and 64-bit-processor architectures and cores targeting

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Comparison Table*

	Agilent LXI Switch/Measure**	NI PXI Switching***
List Price (100 channels)	**$4,779** Uses 2 of 8 slots	$9,190 Uses 5 of 5 slots
List Price (300 channels)	**$9,565** Uses 5 of 8 slots	$21,969 Uses 12 of 14 slots
List Price (500 channels)	**$13,915** Uses 8 of 8 slots	$32,257 Uses 18 of 18 slots
	Features	
I/O to computer	Industry Standard LAN, USB, GPIB	Proprietary PCIe-MXI
Scanning speed	109 chan/sec	140 chan/sec
Size	3U vertical space in rack	4U vertical space in rack
Front panel	Yes	No
Graphical Web interface	Yes	No

**Based on a typical data acquisition application with inputs up to 300V multiplexed to a 6 ½-digit digital multimeter for measurements.*

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***Based on 34980A pricing and data sheet from www.agilent.com/find/34980A on Sept 29, 2006.*
****Based on PXI switch pricing and data sheet from National Instruments Web site on Sept 29, 2006.*

Agilent Technologies

digital-consumer, networking, personal-entertainment, communications, and business applications. MIPS cores include the entry-level MIPS32 4KE core, the flagship 24K and 24KE processors, and the multithreaded 34K core family. The company introduced the fully synthesizable 32-bit 74K processor-core family that can achieve operating frequencies greater than 1 GHz in standard 65-nm-process technology.

NATIONAL SEMICONDUCTOR, WWW.NATIONAL.COM

National Semiconductor's CP3000 connectivity-processor family combines a RISC core with on-chip SRAM and flash memory, hardware-communications peripherals, and an expandable external bus to target embedded-system-communications applications. These applications include automotive telematics, vehicle-network gateways, hands-free car kits, and industrial- and medical-instrumentation and control.

The COP8 flash microcontrollers feature an 8-bit core and as much as 32 kbytes of on-board flash that you can use as data or program storage and that work for more than 100,000 delete/write cycles. The devices offer virtual-EEPROM functions, in-system programming, and integrated analog- and mixed-signal functions for stand-alone and Internet-controlled applications.

NEC ELECTRONICS AMERICA, WWW.AM.NECEL.COM

NEC Electronics America offers highly integrated, low-power microcontrollers with both embedded flash memory and mask ROM for consumer, mobile, medical, industrial, and automotive applications. The 8-bit K0 and K0S microcontrollers have low-power-consumption capabilities and provide integrated peripherals targeting consumer appliances, home-health-care equipment, building-management systems, and industrial controllers. This year, the company expanded its 8-bit all-flash lineup with 78K0/Lx3 microcontrollers for consumer-electronics products.

The V850 series delivers 32-bit processing performance, low-voltage operation, DSP functions, and on-chip peripherals targeting consumer-electronics products. The V850E/IG3 and V850E/IF3 microcontrollers target inverter-control systems in consumer products, such as air conditioners, refrigerators, and washing machines.

The company expanded its 16- and 32-bit support for industrial and office applications, such as security systems, utility meters, and scanners and printers with the 78K0R/Kx3 and V850ES/JJ3 microcontrollers. And the company continues to support its 64-bit MIPS-based VR Series microprocessors that target embedded digital-consumer devices.

NXP, WWW.STANDARDICS.NXP.COM/MICROCONTROLLERS

new

Philips Semiconductors founded and spun off NXP Semiconductors this year. NXP offers more than 100 ARM7-, ARM9-, and 80C51-based microcontrollers. NXP's LPC3000 and LPC2000 ARM-based families include integrated peripherals, such as Ethernet, device and host USB OTG (On-The-Go), CAN (controller-area-network), and many serial-communications peripherals. NXP recently acquired the ARM9- and ARM7-based BlueStreak LH7A and LH7 series from Sharp Microelectronics (www.sharpsma.com). The LH7 and LH7A series feature high-performance integrated LCD controllers and available system-level systems.

OKI SEMICONDUCTOR, WWW.OKISEMI.COM/US

Oki's Advantage Microcontroller family comprises ARM-core-based products ranging from the ML671000 with a built-in USB controller to the high-performance, 120-MHz ARM946E-based 6200 Series with instruction and data caches. Oki's 4060, 4050, 675K, and 674K series ARM7 Advantage microcontrollers offer variations in frequencies, memory sizes, caches, features, and packages.

PA SEMI, WWW.PASEMI.COM

new

PA Semi offers high-performance, low-power 64-bit Power Architecture processors with highly integrated peripheral functions. The PA6T-1682M PWRficient processor implements a coherent, ordered-crossbar interconnect, two 2-GHz Power Architecture processor cores, 2 Mbytes of L2 cache, two DDR2-memory controllers, multichannel DMA, and hardware-acceleration engines. The PA6T-1682M targets networking, telecom, storage, single-board-computer, industrial, and military-aerospace applications.

PMC-SIERRA, WWW.PMC-SIERRA.COM

PMC-Sierra's MIPS-based processors target metropolitan-transportation, storage-area-networking, wireless-equipment, VOIP (voice-over-Internet Protocol), Internet-routing-equipment, enterprise-switch, and multifunction- and laser-printer applications. PMC-Sierra's family of 64-bit, integrated, 1-GHz CPUs delivers high performance, low latency, and low power consumption with integrated standard interfaces. The MSP (multiservice-processor) family targets use in CPE (customer-premises equipment), such as wired and wireless VOIP-terminal adapters, home gateways, voice-enabled routers, and NAS (network-attached storage).

RABBIT SEMICONDUCTOR, WWW.RABBIT.COM

Rabbit Semiconductor, a Digi International company, provides high-performance, 8-bit microprocessors and development tools for embedded control, communications, and Ethernet connectivity. Rabbit offers embedded-design systems, including low-cost development kits, and technical support for both hardware and software.

RAMTRON, WWW.RAMTRON.COM

Ramtron's new FRAM (ferroelectric-random-access-memory)-enhanced Versa 8051 microcontrollers combine a high-performance system on chip with nonvolatile FRAM. FRAM writes at bus speed with virtually unlimited endurance and low power for guaranteed data integrity in systems that require rapid and frequent writes and low power consumption. Versa 8051 microcontrollers let designers upgrade 8-bit applications without a costly investment in a new architecture and code.

The new VRS51L3174 with 8 kbytes of FRAM comes in an industry-standard 44-QFP for easy device migration. The recently released VRS51L3072 with of 2 kbytes of FRAM and the VRS51L3074 with 8 kbytes of FRAM are available in 64-pin QFP packages. The VRS51L3x74 targets embedded data-acquisition, sensor, and control systems in industrial; motor-control; imaging; security; automotive; metering; data-collection, -storage, and –processing; computer and peripheral; measurement; and medical applications.

RENESAS TECHNOLOGY, WWW.RENESAS.COM

Renesas' processor offerings for embedded systems extend from low-power, 8- and 16-bit microcontrollers to high-performance, 32-bit microprocessors. The low-power, 8- and 16-bit microcontrollers in the R8C/Tiny, H8/Tiny, and H8/SLP series target consumer applications, and the 16-bit M16C, 32-bit M32C, and 32-bit RISC SuperH families target automotive and consumer applications. The H8 family meets the needs of PC and server applications, and the 32-bit RISC SuperH family targets designs requiring higher performance and multimedia capabilities. Renesas also offers AE-series devices for smart-card applications and R-Secure devices for systems needing robust embedded-security functions.

The new devices in the H8SX/1622, 1638, and 1648 groups offer as much as 1 Mbyte of on-chip flash memory and a deep software-standby mode. The H8S/2378-based direct-

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drive LCD handles QVGA (quarter-video-graphics-array) panels while performing real-time control tasks. The R32C/118 devices provide a single-precision floating-point unit. The SH7205 and SH7265 dual-core SuperH microcontrollers deliver 960-MIPS CPU performance and 800-MFLOPS (million floating-point operations per second) for advanced consumer, industrial, and car-audio applications.

SAMSUNG ELECTRONICS, WWW.SAMSUNGSEMI.COM

Samsung offers 16- to 32-bit processors targeting handheld-system applications, including smart phones, VOIP (voice-over-Internet Protocol) phones, portable GPS (global-positioning-system) devices, gaming systems, and PDAs (personal digital assistants). Samsung's mobile-application processors features ARM920T-, ARM926EJ-, and ARM1176-based RISC cores. Samsung developed the processor family using CMOS-standard cells and a memory compiler; the family adopts the AMBA (advanced-microcontroller–bus architecture), and the newer ARM1176-based systems use an advanced multilayer AXI (advanced-extensible-interface)-bus architecture.

SEMTECH, WWW.SEMTECH.COM

Semtech acquired Xemics in 2005 and offers that company's 8- to 22-bit microcontrollers that interface sensors and radio transceivers and target autonomous, battery-operated, wireless devices. These devices operate at a constant one instruction per clock that is independent of the type of operation and addressing mode.

The Radio Machine device for ISM (industrial/scientific/medical)-band-transceiver interfacing includes a low-power RISC core with the BitJockey, a serial interface for radio protocols, and a UART. Semtech offers tools and application notes for radio development. The Sensing Machine device for sensor interfacing includes a low-power RISC core with the high-resolution ZoomingADC sigma-delta ADC and a programmable preamplifier.

SILICON LABORATORIES, WWW.SILABS.COM

Silicon Labs' 8-bit, mixed-signal microcontrollers integrate configurable, high-performance analog; a high-speed, pipelined 8051 core; in-system-programmable flash memory; and on-chip JTAG-based debugging.

The company's precision mixed-signal, CAN (controller-area-network), small-form-factor Ethernet and USB microcontrollers target industrial, consumer, automotive, motor-control, medical, and communications applications. The family combines high-precision analog data converters having 10 to 24 bits of resolution with a high-throughput 8051 CPU.

The company recently entered the automotive-microcontroller market with the C8051F52x and C8051F53x family.

SILICON STORAGE TECHNOLOGY, WWW.SST.COM

Silicon Storage based its FlashFlex family of 8-bit-microcontroller products on the company's SuperFlash CMOS-semiconductor-process technology. These microcontrollers implement the 8051 instruction set and are pin-for-pin-compatible with standard 8051 microcontroller devices. FlashFlex devices are available in single- or dual-block configurations, and they are ISP (in-system-programmable) and IAP (in-application-programmable). These microcontrollers target consumer, communication/wired, imaging and video, audio, industrial, and motor-control applications.

STMICROELECTRONICS, WWW.ST.COM

STMicroelectronics offers 8- and 32-bit microcontrollers and application-specific devices targeting motor-control, USB, and CAN (controller-area-network) applications. The company offers development tools, training courses, consulting services, and Web support. The company based the ST7 core on an industry-standard 8-bit architecture and extended the architecture to improve support for high-level language programming and to provide additional interrupt-handling features. The ST7 microcontroller family targets smart-appliance, motor-control, automotive-body, home-automation, or any of today's emerging microcontroller applications. STMicroelectronics' 32-bit ARM-processor offerings include the STR7 with an ARM7TDMI core, STR9 with an ARM966 core, and the new STM32 with a Cortex-M3 core.

STRETCH, WWW.STRETCHINC.COM

Stretch provides software-configurable processors for computationally intensive applications. Stretch's latest processors, the S6000 series, targets high-speed video and image processing. Thus, the company has developed two reference-design kits using S6000 family software-configurable processors, a PCIe (Peripheral Component Interconnect Express) DVR (digital-video recorder), and an IP (Internet Protocol) camera.

TENSILICA, WWW.TENSILICA.COM

Tensilica offers two families of 32-bit-processor cores. Tensilica's Xtensa processors are configurable, extensible, and synthesizable. The company's Xtensa processor generator au-

tomatically matches all associated software with any changes to the processor.

The Diamond Standard processor line of optimized processors ranges from a small, energy-efficient controller to audio and video processors and a fast, high-end processor. Tensilica based the Diamond Standard family on the Xtensa configurable-processor architecture, and most members feature direct interface ports and queues for high-speed I/O.

TERIDIAN, WWW.TERIDIAN.COM

Teridian Semiconductor's analog- and mixed-signal ICs target automation, networking, and secure-access applications, such as smart-card readers, VOIP (voice-over-Internet Protocol) gateways, set-top boxes, POS (point-of-sale) equipment, utility meters, and factory-floor automation. Teridian recently simplified three-phase-meter design and reduced system cost 40% with the 71M6523 three-phase-metering SOC (system on chip). The single-chip 71M6523 delivers antitamper neutral-current-measurement accuracy of 0.4%, allowing the detection of small energy theft and surpassing alternative approaches by a factor of two. The company also introduced the 72S1217F 8-bit PIN (personal-identification-number)-pad smart-card-reader SOC and the 73S1209F and 73S1210F turnkey smart-card-reader ICs. These devices join the 73S1215F, which enabled the industry's first USB-connected smart-card readers.

TEXAS INSTRUMENTS, WWW.TI.COM

TI announced the T2012 and the MSP-Mojo target boards for the eZ430 development tool. The T2012 features the MSP430F2012 ultralow-power microcontroller with an integrated high-performance, 200k-sample/sec, 10-bit ADC. The company also introduced its eZ430-F2013 development tool.

TI announced volume availability of the MSP430FG461x series of ultralow-power microcontrollers, targeting industrial sensing applications, including portable medical systems. TI also announced the availability for sampling of its 16-MHz MSP430F47x4 ultralow-power microcontroller for one-phase and multiphase metering.

TILERA, WWW.TILERA.COM

Tilera offers high-performance multicore processors targeting embedded networking, security, and multimedia-processing applications. The Tile processor family targets applications requiring intensive packet processing for layers 2 through 7 and for HD (high-definition) video applications.

The Tile64 processor SOC (system on chip) has 64 full-featured processor cores plus a rich suite of system-integration blocks. The device includes 5 Mbytes of cache, and each processor core can independently run a full operating system, such as Linux.

Tilera based the Tile64 family on a tiled multicore architecture with a mesh-based on-chip interconnect. This architecture delivers as much as 32 Tbps of interconnect bandwidth between the cores and allows scaling the architecture beyond hundreds of cores.

TOSHIBA AMERICA ELECTRONIC COMPONENTS, WWW.TOSHIBA.COM/TAEC

Toshiba offers highly integrated 8-, 16-, and 32-bit CISC microcontrollers with embedded SuperFlash1 memory and 32- and 64-bit, MIPS-based TX RISC microprocessors. TX RISC devices suit calculation-intensive applications that require large memory capacity and DSP-like functions.

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handheld information systems, printers, calculators, toys, range finders, white goods, and thermostats; home-security systems; HVAC; and instrumentation, mirror, and air-bag automotive systems. A focus product, the high-performance, 32-bit, 80-MHz TMP92CZ26AXBG microcontroller, has a built-in LCD controller and a 288-kbyte embedded RAM. It is appropriate for general-purpose applications and electronic systems requiring 32-bit performance to drive an LCD and a USB interface.

TRANSMETA, WWW.TRANSMETA.COM

Transmeta no longer manufactures microprocessors, but it offers its microprocessor IP (intellectual property) for license. The Crusoe processor targets extreme low power with a balance of performance and cost. Crusoe supports Microsoft (www.microsoft.com) and Linux embedded operating systems and other real-time operating systems. Transmeta's second-generation Efficeon processor expands on the performance range that Crusoe offers.

UBICOM, WWW.UBICOM.COM

Ubicom develops communications and media processors as well as software for home networking. Ubicom's chips and software efficiently and with low latency move media around the home. The company's technology targets wireless routers, Internet-access devices, access points and bridges, print servers, and networked audio and video players.

VIA TECHNOLOGIES, WWW.VIA.COM.TW

Via processors target x86-based personal electronics and embedded devices with feature-rich digital-media chip sets. Via divides its processors into five product families that it bases on power-consumption and performance criteria ranging from fanless operation to power-saving capabilities for battery-operated mobile devices. The families are the C7 and C7-M mobile, the fanless Luke, the Eden-N and fanless Eden ESP, the C3-M mobile, and the C3 processors.

XILINX, WWW.XILINX.COM

Xilinx offers embedded processors, FPGA platforms, and development tools that target aerospace and defense, wired- and wireless-communications, automotive, audio- and video-broadcast, industrial-control, test-and-measurement, and consumer applications. The Virtex family of high-performance FPGAs includes the PowerPC 32-bit hard core. The configurable, general-purpose, 32-bit MicroBlaze soft core is available for use with the Spartan family of low-cost FPGAs and Virtex-platform FPGAs.

ZILOG, WWW.ZILOG.COM

Zilog offers 8-, 16-, and 32-bit microprocessors. This year, the company introduced three new product families and completed the transition to a fabless-semiconductor model. Zilog's Zbase remote-control code database, Crimzon products, and engineering services support designers of universal remote-control devices. Zilog launched its first 32-bt ASSP (application-specific standard product), the ARM-based Zatara family of products, to meet the banking industry's requirement for all POS (point-of-sale) systems to be PCI (payment-card-industry) PED (PIN-entry-device)-compliant. Zatara devices also target adjacent markets, such as PIN (personal-identification-number) pads, ATMs (automatic teller machines), gas pumps, kiosks, and other POS terminals. Zilog also introduced the new high-performance eZ80AcclaimPlus! products for networking connectivity.EDN

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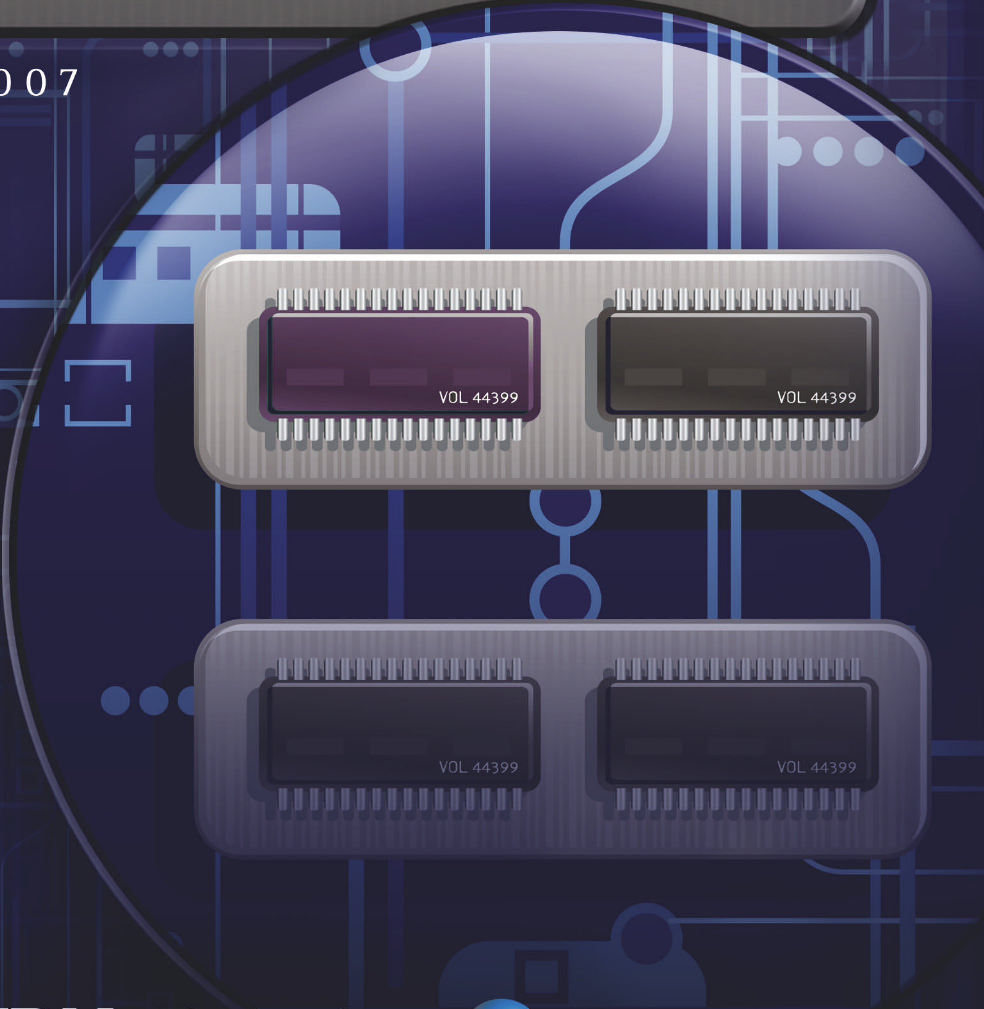

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FORGERIES IN SILICON

Exposing the Deceptions of Component Counterfeiters

Meeting the COUNTERFEITING CHALLENGE

A LETTER FROM THE EDITOR

While most people are familiar with the trafficking of DVDs, pharmaceutical drugs, and brand-name purses, few are aware of the tremendous counterfeiting business that has arisen in the electronics industry. According to Fremont, California-based Alliance for Grey Market and Counterfeit Abatement (AGMA) (www.agmaglobal.org), up to 10% of technology products sold worldwide are counterfeit, amounting to on the order of $100 billion in sales revenues.

Robin Gray, executive vice president of the National Electronics Distributors Association (NEDA), says its members are concerned that "counterfeiting may become the number one industry issue in the coming years." Counterfeiting electronics components has become especially prevalent as contract manufacturing increases because, to put it literally, it is much harder to spot a fake processor than it is a fake purse. Unfortunately, while a fake purse may make you look bad if others recognize it, counterfeit electronics components can result in equipment failure that exposes OEMs to substantial business losses.

Counterfeiting used to be more challenging before the rise of outsourced contract manufacturing. In order to avoid inventory taxes, many OEMs have relinquished even the procurement of components, instead "buying" components from the manufacturer or supplier and owning them for perhaps seconds before selling them to a procurement company or factory taking on this task.

When you outsource production and procurement, quality control is managed by the contract manufacturer. Many of these manufacturers have nothing to lose, except perhaps your next job. And when they are outside the jurisdiction of the United States court system, protecting yourself becomes quite a different problem. Contract enforcement in China and India is difficult, and many companies simply don't have the resources to wage an overseas legal battle. As Gray puts it, "Counterfeiting is going to impact the outsourcing movement that has occurred over the past decade and may well result in OEMs revisiting that philosophy." As counterfeiting becomes more prevalent, and as its associated risks and losses continue to increase, the promised returns of outsourcing become significantly less attractive.

Certainly it is exciting when a contract manufacturer offers up its own sources, especially when you consider the lower BOM. However, if these savings are based on the use of counterfeit components, they may come at a high cost, measured in terms of product returns, increased liability risk, and brand damage.

It is important to note that counterfeiting is not isolated to the electronics industry. This means that legitimate players will not find themselves without a voice. In fact, manufacturers across diverse industries are working together to develop technology, regulations, and awareness of the impact of counterfeiting on consumers.

Part of meeting the counterfeiting challenge is understanding that you may find yourself working with counterfeiters even when you think all of your sources are reliable. The key to protecting yourself, then, is being aware of the different forms counterfeiting can take, understanding the risks involved as pertains to your particular application, and being willing to take the steps available to you to mitigate these risks. ■

Nicholas Cravotta is an industry expert and a professional writer with more than two decades experience and more than 150 published articles. He also holds two patents.

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Reed Electronics Group
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Reed Business Information
225 Wyman Street, Waltham, MA 02451
Phone: (781) 734-8000
www.edn.com

EDN Worldwide
Alan Robinson, Group Publisher
Phone: 408-345-4450
Fax: 408-345-4400
aarobinson@reedbusiness.com

Barbara Couchois
National Sales Director
barbara.couchois@reedbusiness.com

Cindy Fitzpatrick, Director
EDN Custom Programs & Solutions
cfitzpatrick@reedbusiness.com

Regina Twiss, CPS Manager
reginatwiss@comcast.net

Special Issue Editor:
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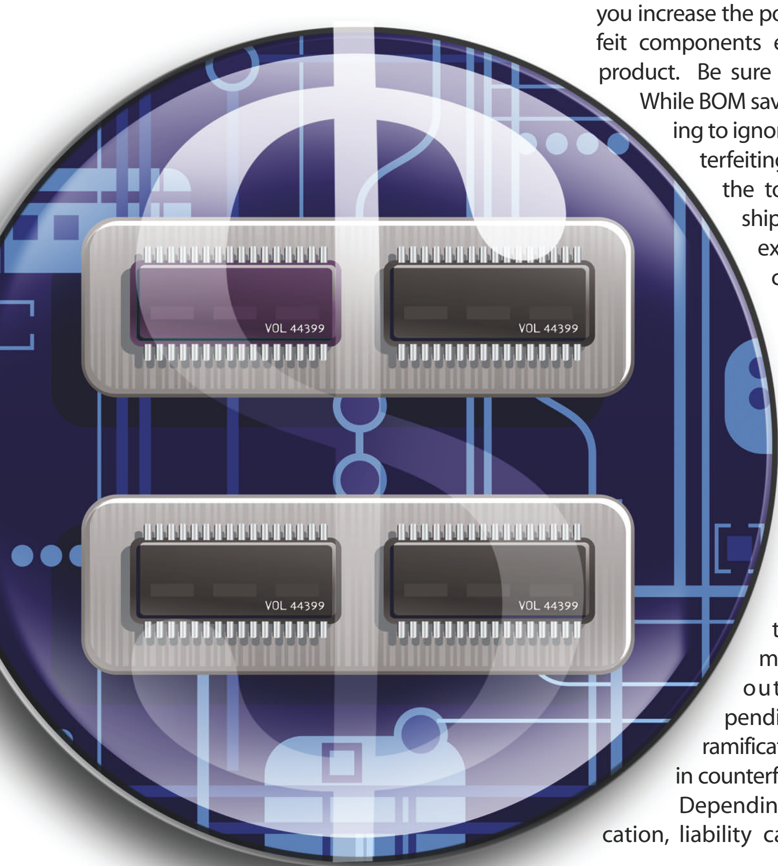
FORGERIES IN SILICON

Exposing the Deceptions of Component Counterfeiters

The HIGH COST of COUNTERFEITING

Overseas contract manufacturers often have their own sources for components, many of them legitimate. After all, these factories want your business over the long term. They offer price savings to be competitive as well as to attract you in the first place, citing 10-20% savings even from authorized suppliers, which can be attributed to lower overhead costs. But if the savings are too low, such as processors at half market price, it's time to become suspicious. After all, if it seems too good to be true, the factory needs to be able to explain why that's the case. If may be worth your while to follow the paper trail for the most likely candidates for counterfeiting (i.e., those with the highest return) to confirm that your procurement agent is being honest with you.

When you outsource procurement through contract manufacturing, you increase the possibility of counterfeit components ending up in your product. Be sure to weigh the risks. While BOM savings make it tempting to ignore the issue of counterfeiting, you need to take the total cost of ownership into account. For example, if you discover that the product you purchased is counterfeit and will not work for you, you may not be able to return it unless you purchased it from an authorized source which offers full warranty protection. In addition, the product may be seized without compensation pending potential legal ramifications for trafficking in counterfeit goods.



Depending upon your application, liability caused by counterfeits can also be a major issue. A failed pacemaker, for example, results in a person's death, so there is no tolerance for counterfeit components there. But even in cases where safety is not an issue, counterfeiting can have tremendous negative impact on returns and/or brand reputation. Consider a resistor causing the failure of a high-ticket item, like a digital TV or media player and forcing a recall. Increasing the number of less-than-robust components in a system increases the chance of failures, and you could see all of your saving evaporate in handling returns. Additionally, each return has the potential of generating negative word-of-mouth, leading to long-term brand erosion.

ROGUES GALLERY

Counterfeits can take a number of different forms, each of which exposes your company to different risks:

Outright fakes. The most commonly recognized type of counterfeiting, fake components are marked as if they were produced by the appropriate manufacturer but in fact have been manufactured by another source (see Figure 1). They bear the trademarks and logos of the original manufacturer and may even perform to spec. The obvious problem with using fakes is that they don't come with the same guarantees that genuine parts do.

Remarked. Remarking refers to components whose markings have been

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altered in some way. These components may be genuine parts, but their part number or other identifying markings have been modified to match that of a more expensive version of the component. For example, a 1.2 GHz processor may be remarked so as to appear to be a 1.8 GHz part or to have a higher memory capacity than it actually has.

Non-compliant. Many OEMs need to maintain compliance with any number of government regulatory bodies, and counterfeiting can jeopardize later certification of products. For example, lead-free components are more expensive to manufacture than those made using lead. However, the two types of components look the same, making it tempting for unscrupulous distributors to sell components as lead-free when in fact they aren't. Use of such components will result in compliance failure, causing substantial delays as well as subject the company to fines, penalties, and even the possibility of having to remove a product from the marketplace.

Recycled. The cost of labor in China and India makes it a profitable endeavor to ship obsolete equipment to these countries for disposal and recycling. However, components may be removed and then sold as new or returned parts without any mention being made of their true source. Even if recycled components are genuine, their quality can vary tremendously. Often acid is used to remove components and delicate leads can be damaged when components are ripped off of boards, resulting in only partial functionality or the higher risk of a later failure.

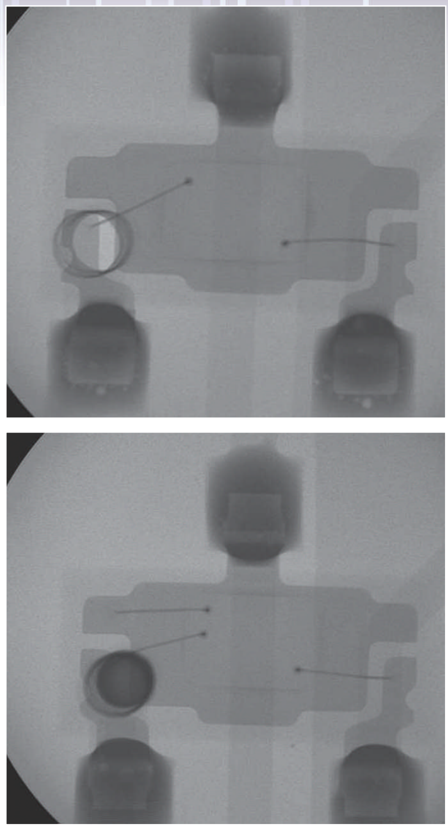

Figure 1: Counterfeit vs. Functioning Component.

Source: Association of Franchised Distributors of Electronic Components, United Kingdom

Less robust. While these components may perform to spec in most ways, the lower cost techniques used to manufacture them may reduce, for example, operating temperature, input voltage ranges, and functionality.

DELAYED FAILURE

One of the extremely debilitating difficulties with counterfeit components is that problems may not arise until equipment has been deployed in the field. Many processors, for example, are speced at a variety of clocking speeds. Through a process called binning, components are tested and those which do not pass the most rigorous tests are rated at a lower clock speed. When components are remarked to a higher clock speed, they may only perform to spec for a short time before failing.

While testing components may not help you determine whether you have genuine components or not, it can verify component reliability (see Figure 2). Testing, however, can be expensive and time consuming, requiring thousands of dollars, depending upon which lab you use and how much testing you have to do. To verify specs, for example, you may decide to test a small sample of the components you receive. The size of the sample and whether you test each shipment of components you receive depends upon the complexity of your system, how many components you have to test overall, and how critical the component is.

Counterfeiters, however, are onto this defense, and may intersperse genuine components in among the counterfeit components in the hopes that you'll select a reliable part for testing and be none the wiser. Additionally, since genuine parts can fail, testing assumes a certain number of failures which can mask the presence of counterfeits. Testing for issues such as whether a component is truly lead-free are even more cost prohibitive. However, if being lead-free is important, your customer may test your completed product when it is too late to change out components.

UNAVOIDABLE EXPOSURE

Typically, the most reliable source for components is a manufacturer-

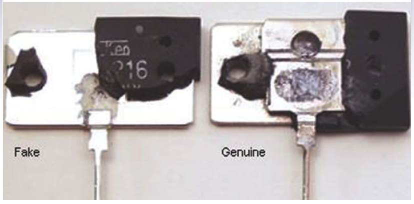

Figure 2: Counterfeit vs. Genuine Sanken Transisitor.

Source: Association of Franchised Distributors of Electronic Components, United Kingdom

authorized supplier which provides full warranty protection as well as product support. Sometimes components are in short supply, however, and you may find that you aren't as high on your supplier's priority list as you thought. If you don't want to slow down your assembly line, you may find yourself having to second source components through the grey market (i.e., unauthorized distributors, brokers, and third parties). To limit your risk in such cases, work with a company that you've done business with in the past or that has a solid reputation.

Many suppliers offer guarantees on components that they provide; be sure they have the financial solvency to back them. If you go through a broker offering no guarantees, you may find yourself stuck with a very expensive bargain. While many manufacturers don't take returns on overstocked inventory, some do offer scrap allowances. This is where the manufacturer pays you to scrap the components rather than return or resell them.

Verification is required for scrapping, and you can even outsource scrapping. Verification of scrapping is not simple, and many "scrapped" components may find their way onto the grey market. Scrapped components can present a real problem for OEMs. While these may be genuine components, they officially don't exist and a manufacturer won't guarantee them.

Even the most careful buyers can find themselves stuck with counterfeit components. For example, it is possible to acquire counterfeit components from authorized suppliers who accept returns. Consider the case where a company has sourced parts from an authorized supplier and grey market source. Some of the grey market components may be returned as well, introducing potential counterfeits into the supply. Certainly, authorized suppliers are expected to guarantee these components, but you may still encounter undesirable returns, liability, and brand damage in the meantime. It's a good idea to be aware of any supplier's return policies as well as the limits of their guarantees.

To mitigate their own liability, suppliers will attempt to verify that they are getting back the actual components they sold you, using techniques such as requiring original packaging and using date coding to confirm that the components returned are the ones originally shipped. These measures are not foolproof, but they offer a certain level of assurance, and distributors can implement them without adding unreasonable overhead. Ideally, if you acquire a component from multiple sources, it is best to keep them separated or have some way of separating them if you need to so you can return them to their original sources. This is a challenging decision to make, given the already thin margins contract manufacturers operate under since co-mingling components is far more cost effective than managing multiple bins. However, it may make sense to separate out critical, expensive, or at-risk components while co-mingling the rest. ■

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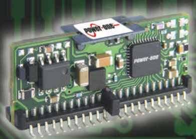
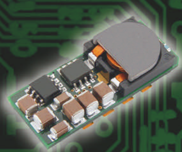


Z-Series Digital POLs



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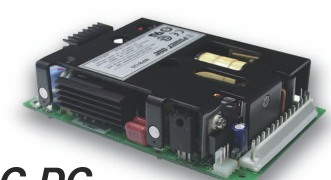
CompactPCI	AC-DC and DC-DC in 3U and 6U form factors.

AC-DC Front Ends



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BY BOB KIRK • AMI SEMICONDUCTOR

FPGA-prototyping and ASIC-conversion considerations

CONVERTING YOUR FPGA TO AN ASIC YIELDS MANY BENEFITS. HERE'S A LOOK AT HOW DESIGNERS CAN MAXIMIZE THOSE BENEFITS AND MAKE THE TRANSITION AS QUICK AND SEAMLESS AS POSSIBLE.

The capacity and capability of modern FPGAs support the implementation of many digital systems, making FPGAs the platforms of choice for developing, prototyping, and deploying digital logic. Depending on the requirements of your system, using FPGAs may not be the best approach for field deployment. Factors such as high unit cost and high power consumption may require deployment with an ASIC device. Still, designing with an FPGA makes more sense, and, by paying attention to a few details up-front, the conversion to an ASIC device need not be difficult. Those details include power supplies, packaging, boundary-scan testing, and other considerations.

DEVICE POWER SUPPLIES AND PACKAGING

It may seem odd that power supplies are at the top of the list. But they can be the sources of the greatest potential cost savings to you as a system designer. The drive to ever-higher FPGA logic densities and speeds has pushed FPGAs into leading-edge semiconductor processes, which operate at lower and lower voltages. The latest FPGA devices fabricated in 65-nm technology have core logic operating at 1V. But does anyone really need to build an ASIC device in 65-nm technology to offer the same performance as an FPGA? The answer is clearly no; thus, the cost of building an ASIC in a 65-nm process is unwarranted. Depending on the system requirements, you may be able to convert that 65-nm FPGA into 90-, 130-, 180-, or even 350-nm ASIC technology. Generally, the larger the technology, the less capability and performance available, but the cost correspondingly decreases. Why pay for a rocket ship when all you need is a car?

The problem comes with the fact that larger geometry process technologies run at higher operating voltages. If you can't easily change out a 1V core power supply for a 1.2, 1.5, or 3.3V supply, then you may be stuck with converting to a process technology that is more expensive than you need.

The first and most important thing you can do is design the power-supply scheme for the FPGA core supplies in such a way that you can later easily change to another voltage. This approach typically means using a dedicated and isolated power plane for the FPGA core-logic supply—a task you may need to perform anyway for FPGA-supply-noise isolation—and arranging the regulator so that you can either swap it out or change a component value.

When it comes to packaging, the cost is often higher than that of silicon. This fact is especially true for high-pin-count packages and flip-chip devices. What can you do to reduce package costs? First, FPGA devices, with their high power consumption, often require expensive, "thermally enhanced" packages. During conversion to a lower power ASIC, the simplest thing to do is to shift to a plastic package with the same footprint.

Designers often use large FPGAs to ensure adequate logic and memory resources. But do you need all those pins? If not,

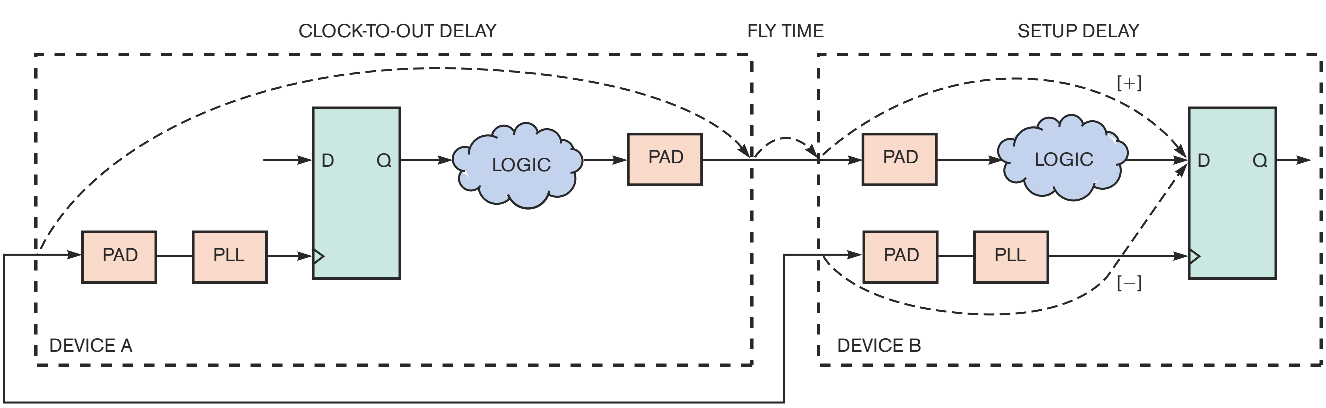


Figure 1 Two devices work together with the timing budget.

then you might want to consider switching to a smaller package when converting to an ASIC. You may have noticed that some FPGA families support vertical-package migration. This approach lets you start with a small package and move to a larger package if necessary, because the pin assignments of the smaller package are compatible with those of the larger package. Consider putting that principle into practice but in reverse: Use the large FPGA package, but define the pinout to avoid using the I/O pins in the outer rings. Then, when you convert to an ASIC, you can use a smaller package but still have a package that is footprint-compatible with your board. You can employ a lot of schemes in prototyping, including the use of an FPGA daughterboard. Whatever approach you use can lead to tremendous cost savings if you can reduce the package pin count.

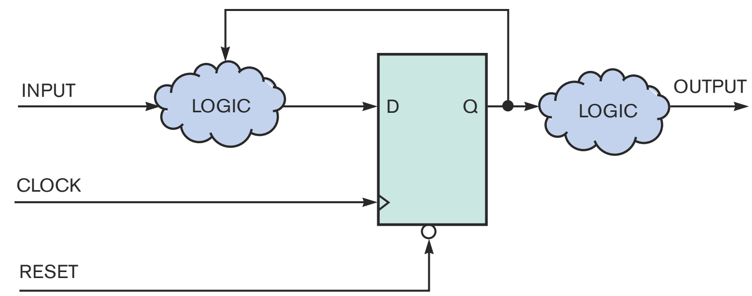


Figure 2 The best-case scenario is to have one common clock that goes to all flip-flops and one common reset line that goes to the reset pin or the set pin of each flip-flop.

BOUNDARY-SCAN-TEST DEPENDENCIES

Do you care about how JTAG (Joint Test Action Group) testing works? Probably not, but your test people do. Dependencies on how JTAG testing works can have a big impact on the cost savings you obtain when you convert an FPGA to an ASIC. The problem is that FPGAs support JTAG boundary-scan testing on all the standard I/O pins, whether you use the pins or not. When developing the board-level test, test programs shift data through the boundary-scan shift register in a way that includes all the pins, even if the circuit does not use some of them. If these unused pins connect to board traces, the JTAG tests may access them as test points. When converting to an ASIC, you must match the form, fit, and function of the FPGA; unused pins become problematic. If you remove them, then boundary-scan test may not work. If you retain them, then the ASIC must have "extra" pins and associated bond pads, just for supporting boundary-scan test.

I/O-bond pads use a lot of silicon area. If you can eliminate the implementation of unused pins, then you can reduce the silicon-die area. You can still put the ASIC device into the same package, but you need not connect all the pins to the silicon die. To put this scenario into perspective, consider that, if 30% of your I/O pins are unused, the silicon die can be as much as 50% smaller, leading to significant cost savings. Work with the test engineers to let them know that the ASIC device does not support boundary scan for unused I/O pins. They may want to mask these pins in test development so that they don't unwittingly use them for critical test points.

To maximize the benefits of FPGA-to-ASIC conversion, you must consider some other items at the board level. As mentioned, you need to maintain flexibility in power-supply voltages; doing so can yield significant power savings. When it comes to the regulator, you may be able to swap in a less expensive device to work with the ASIC. Your FPGA may use EPROM or flash to configure the FPGA device, but, with an ASIC, you can remove the EPROM or flash device from the BOM (bill of materials) for additional cost savings.

With potential regulator changes, smaller packaging, and removal of EPROM/flash devices, you might want to reclaim the unused board space for your application. In this case, using an FPGA daughterboard or a board re-spin might make sense and may be the path to the greatest overall savings. On the other hand, you might not want to mess around with the board and may just want a drop-in replacement.

There are some things you can do in the actual design of the FPGA to facilitate conversion to ASIC technology. IP (intellectual-property) selection is at the top of the list. IP includes simple blocks, such as multiply-accumulate units, memories, and FIFO generators, as well as more complex blocks, such as processors and high-speed serial-I/O SERDES (serializer/deserializer) blocks). The concern with IP is more legal than technical. These blocks usually involve IP-license issues, and many are proprietary to the FPGA vendors. At first glance, the rich catalogs of free FPGA IP seem attractive. However, if you are dealing with medium- to high-volume production for your system, the high cost of the FPGAs can make that "free" IP very expensive.

For these reasons, you need a strategy to avoid getting locked into the FPGA vendor's proprietary IP. Establish a plan for dealing with IP during conversion before you start the design. For example, using native-block memories in the FPGAs is fine, but using the more sophisticated FIFO generators causes the FPGA vendor to create a piece of proprietary IP. You might find it a lot easier in the long run to use a FIFO module from the synthesis vendor or obtain one from your ASIC vendor with permission to use it in the FPGA.

In general, you should try to use synthesizable IP whenever possible. Consider licensing the IP before starting your design and obtaining a license that covers both the FPGA implementation and the ASIC production. It's a good idea to review your IP plans with the ASIC vendor; the vendor may offer suggestions with respect to qualified IP vendors or IP that the ASIC house may have available. It's valuable to negotiate licenses before you get locked into a piece of FPGA IP and have to pay a high price for the ASIC add-on license.

TIMING BUDGETS

Next on the list are some basic documentation items, such as timing budgets. Face it: A NAND gate is a NAND gate. But how fast is the FPGA-NAND gate, and how fast is the ASIC-NAND gate? More important, how fast do you need the NAND gate to be? Timing specifications for the device operating in your system are important. Even more important is an understanding of the overall system-timing budget. **Figure 1** il-

lustrates two devices working together with the timing budget (**Table 1**).

An understanding of all the timing-budget parameters, including margins, can help in the conversion process. If you can use a less expensive ASIC technology, the conversion engineers may need to adjust various timing parameters and still maintain the overall budget. If you don't know your timing budget, you will exceed the FPGA-timing parameters, which may result in unnecessary expense. Other documentation items can also be helpful. It's important to annotate anything that is special about the design, such as any design tricks you used, special timing requirements, start-up requirements, power-down modes, and the like. This information helps the conversion team ensure that your device will function as you intend.

TABLE 1 SYSTEM-TIMING BUDGET

Parameter	System-timing budget (nsec)
T_clk-to-out	2.5
T_fly	2
T_setup	2
T_jitter	0.1
T_noise	0.2
Total time	6.8
Clock period	8
Margin	1.2

For conversion, the starting point will most likely be your RTL code. It's helpful if the code is well-organized and well-documented. You must also supply synthesis scripts and timing constraints. In some cases, you may need to supply part or all of the design in netlist format. Again, organization, scripts, and timing constraints are helpful. Depending on the nature of the design, it may be desirable to supply simulation testbenches to validate the conversion, perform power simulations, or both. For a testbench to be useful, you must pay attention to whether it includes a capture of the supplied stimulus and expected response. The best way to supply this information is to use a VCD (vector-change-dump) file, which captures data whenever a pin changes its value. The data capture must have accurate timing, so it's critical to run the capture simulation with "assignable-delay mode," or full timing accuracy. Zero- or unit-delay modes do not provide accurate timing values in the captured-pin data files.

CONFIGURATION AND START-UP

Unlike FPGAs with their long programming and configuration sequence, ASICs are essentially instant-on parts. However, when planning your FPGA design, you should pay some attention to this area. If the system depends on any of the FPGA-programming features or signals, then the ASIC must perform those same functions. Because your design does not directly include the configuration features that come with the FPGA, issues can potentially crop up. The best approach is to avoid any dependencies in the first place. Potential dependencies include watching "done" pins as part of a successful programming monitor or as part of a system-reset release or another start-up sequence. But, if you want to ensure that a timing generator has locked, then it makes sense to formally bring the lock signal out to a pin. Another case to watch out for is daisy-chaining the configuration stream through multiple FPGAs, especially if you plan to leave any of the devices as FPGAs and not convert them into ASICs.

Another start-up factor to consider is the proper handling of the PORs (power-on resets), which are highly analog. You cannot expect an ASIC POR to behave exactly the same as the FPGA POR. You can't even expect PORs from different FPGA-silicon-manufacturing lots to be exactly the same. It's good system-design practice to have only one device on the system generate a POR signal for systemwide use. This approach prevents potential time-sequence issues and provides reliable system start-up. The FPGA or converted ASIC can be the POR source, but, if so, it should be the only source.

MEMORY INITIALIZATION

Memory initialization is unique to FPGA architectures and provides a simple starting basis of, say, all zeros, for running algorithms, state machines, and so on. It's also an easy way to load in constants, such as filter coefficients. The problem is that ASIC memories power up to an unknown state. You can deal with this problem in various ways. One proven and viable way is for the ASIC-conversion vendor to build initializable memories. Another way is to add some dedicated soft logic or wrapper logic to your design that initializes the memory at start-up. The third and, perhaps, easiest way is to design your system so that it does not depend on memory initialization. To the extent you can make your design not depend on unique FPGA features, your design becomes all the more portable and opens the door to more conversion options and quicker conversion.

Good design practices make conversions smoother and translate into shorter time to market. A review of design practices reveals some hidden conversion issues. Designers often learn that synchronous design is a good approach, and, in the context of conversions, it is, because it makes the design largely independent of logic-gate timing. However, long logic paths may be too slow, and ASIC and FPGA logic gates do not yield the same performance. Even in the same architecture and technology, it is difficult to match delays, so designers add margin. Changing from, say, a 65-nm FPGA to a 130-nm ASIC is also difficult. The best-case scenario is to have one common clock that goes to all flip-flops and one common reset line that goes to the reset pin or the set pin of each flip-flop (**Figure 2**).

However, in many real-world designs, you must deal with multiple incoming clocks. When this scenario happens, you must focus on anywhere that two clock domains interact. Assume the clock signals can change at any time with respect to each other and use carefully thought-out strategies that do not depend on the technology you use. This approach may include using metastable protection flip-flops with various handshake protocols or independently clocked FIFO buffers. This approach is critically important because simulations and even FPGA prototyping may not reveal problems when the delays of various gates change from one implementation to another.

As a corollary, your approach should not include any internally generated or derived clocks or reset signals. Such signals have implied relationships and skews between each other, which may change between implementations. The most common situation is clock gating that you insert to reduce clock-switching power. You may have used this approach in the FPGA implementation to reduce the FPGA's overall high power consumption; however, you may not even need gated clocks in the ASIC implementation because the overall ASIC power consumption is significantly less. In most cases, using a

clock-enabled flip-flop is the simple design alternative to gated clocks. But if you must gate clocks, be sure to document each case, why you need it, and how you know it will work in all cases. Then, review each case with the conversion team.

Other good design practices include adding proper dead-state handling in finite-state-machine design, avoiding latches, and avoiding delay dependencies. These practices aim to make the design as independent of technology characteristics as possible. To put it in perspective, FPGAs tend to have slow gate delays. The logic gates are not slow; the look-up-table implementation can lead to some fast complex-logic functions. However, the programmable interconnect is slow, meaning that a combinational-logic gate that generates a small glitch in an ASIC may cause different behavior in an FPGA. The slow FPGA interconnect may act as a lowpass filter and attenuate the glitch, whereas, in the ASIC, it may speed through to the next gate. If that signal drives the clock pin of a flip-flop, you could have a problem. This reason shows why synchronous design is a good practice: No combinational-logic gates exist on any clock or reset signal, avoiding the problem altogether.

Another practical side effect of following synchronous-design practices is that doing so makes it much easier to test the converted ASIC. Usually, designers employ one or more DFT (design-for-test) strategies, which involve automatic or semiautomatic insertion of test logic and algorithmic generation of a manufacturing-test program. DFT tools work best on circuits that follow good design practices. The use of multiple or asynchronous clocks, multiple clocks, latches, and delay dependencies generally reduces test coverage.

FPGAs are clearly the way to go for prototyping, and, by following these simple suggestions, you can not only maximize your cost savings by converting to an ASIC, but also shorten the conversion time and be confident that your design will function as you intend.

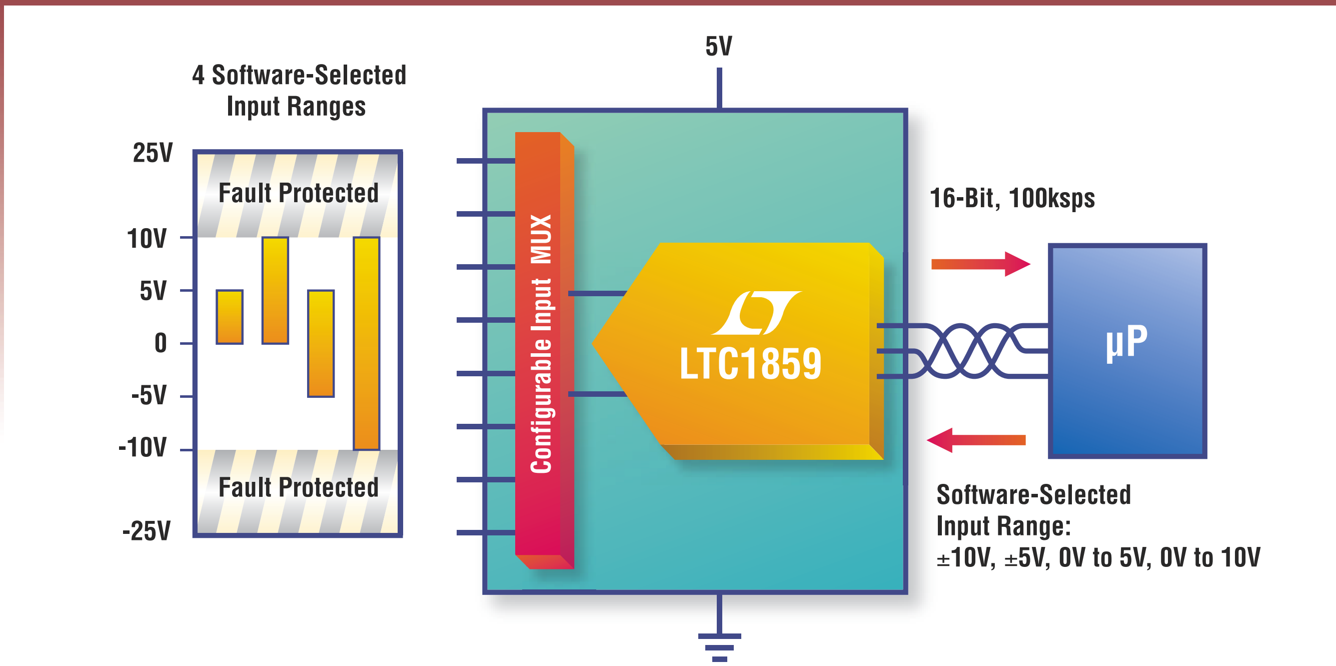
Consider consulting with your ASIC vendor before you start the design. The vendor should be able to give you additional pointers and guidance about design to make the conversion seamless. This suggestion is especially important if you have never been involved in an ASIC development. Although you may think that all logic gates are created equal, FPGAs and ASICs are not exactly the same. It is a good idea to select an ASIC vendor before you start the FPGA design and at least work out a preliminary plan.

A well-thought-out conversion plan maximizes cost reductions by targeting the appropriate ASIC platform, determining the appropriate package, and defining the pinout. It reduces conversion issues by managing IP-licensing issues up-front and determining how you will convert unique FPGA features or whether you should avoid them. The plan should also tackle which design practices you should follow and which you should avoid to improve the overall design quality. **EDN**

AUTHOR'S BIOGRAPHY

Bob Kirk is the director of strategic marketing in the communication-high-voltage-products group at AMI Semiconductor. He holds bachelor's degree in electrical engineering and computer science from the University of Santa Clara (CA). Reach him at bob_kirk@amis.com.

16-Bit, 8-Channel ADC with Software-Selectable Input Span



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LINEAR TECHNOLOGY DESIGN NOTES

6-Channel SAR ADCs for Industrial Monitoring and Portable Instruments

Design Note 426

Guy Hoover and Steve Logan

The 14-bit LTC2351-14 is a 1.5Msps, low power SAR ADC with six simultaneously sampled differential input channels. It operates from a single 3V supply and features six independent sample-and-hold amplifiers and a single ADC. The single ADC with multiple S/HAs enables excellent range match (1mV) between channels and channel-to-channel skew (200ps).

The versatile LTC2351-14 is ideally suited for industrial monitoring applications such as 3-phase power line monitoring to ensure line voltage compliance, portable power line instrumentation, power factor correction, motor control, and data acquisition. These applications may be battery powered, and it is here that the LTC2351-14's low power and small size are desirable. Power consumption is a mere 16.5mW, which extends battery life. The 3-wire serial interface means fewer pins than parallel output devices, allowing the LTC2351-14 to fit in a 32-pin, 5mm × 5mm QFN package.

Power Line Monitoring Application

Figure 1 shows a typical power line monitoring application. Current is sensed by a CR Magnetics CR8348-2500-N current transformer. An LT1790-1.25 biases the output of the transformer to the middle of the LTC2351-14 input range, giving the inputs maximum swing. A 6:1 transformer and 41:1 attenuator scale the line voltage, and the transformer output is similarly biased.

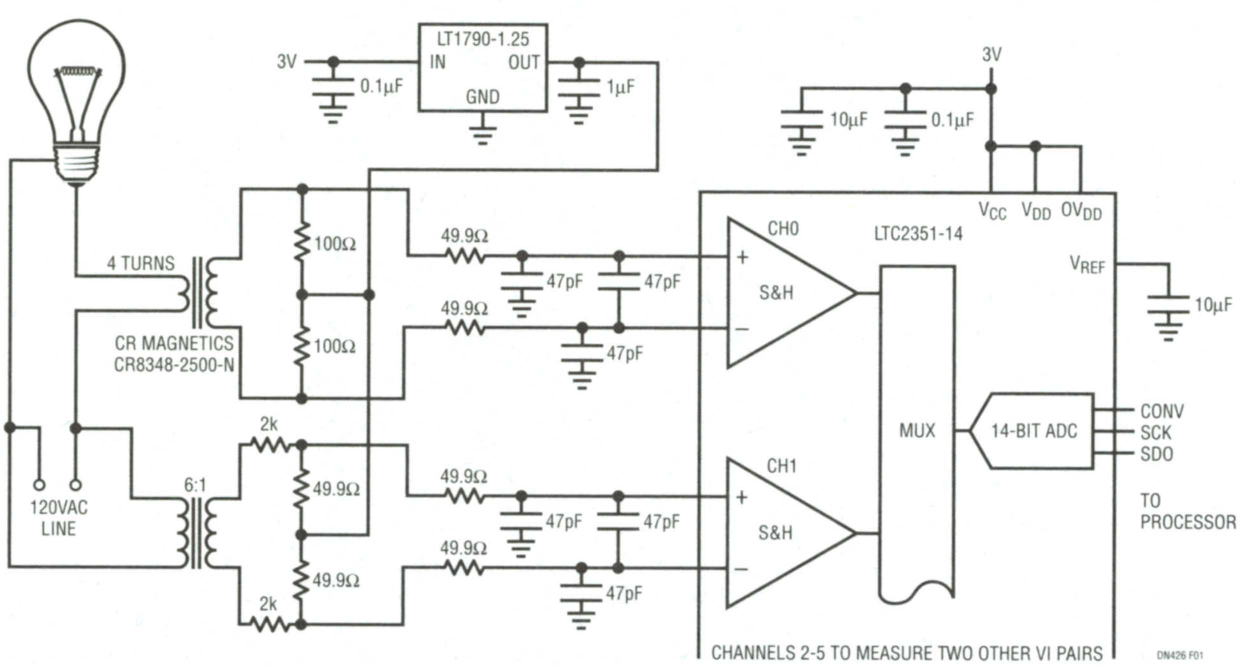

Figure 1. Typical Power Line Monitoring Application

Figure 2 shows the AC line voltage in Linear Technology's Mixed Signal lab. The flattened peaks are typical of the voltage in an office building where many of the loads are nonlinear, such as computer power supplies. Figure 3 shows the current through a 50W incandescent bulb. Figure 4 shows the current through a 15W compact fluorescent bulb, and Figure 5 is the current through a 4W LED-based bulb. The 5MHz full linear bandwidth of the LTC2351-14 allows analysis of high frequency components of the line voltage and current, limited in this case by the bandwidth of the sense transformers.

Conclusion

With PCB real estate getting tighter and designers always searching for lower power ICs, fast data acquisition can be a challenge. The LTC2351-14 and other low power SAR converters make it possible to optimize solution size, power and cost.

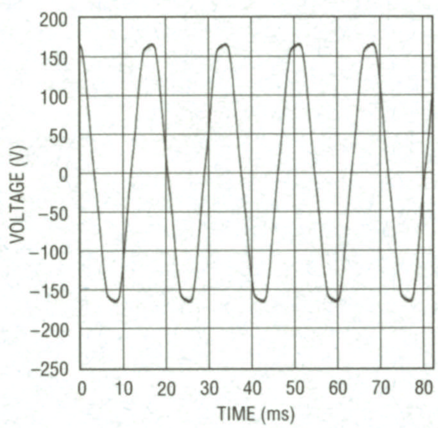

Figure 2. Line Voltage

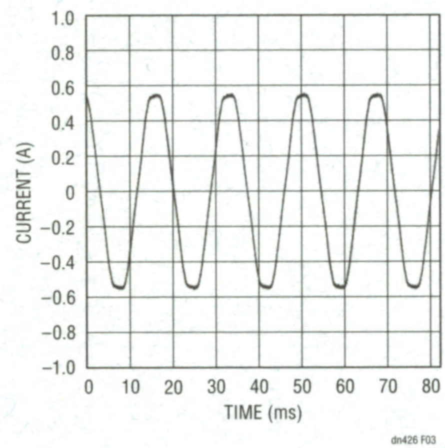

Figure 3. 50W Incandescent Bulb Current

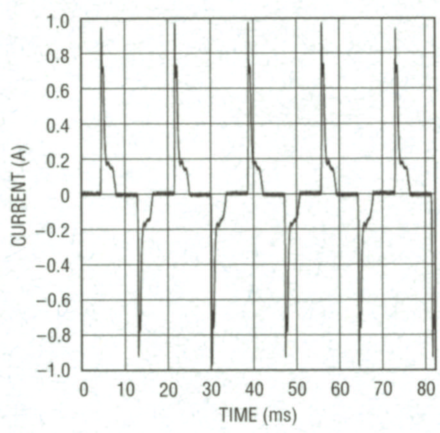

Figure 4. 15W Compact Fluorescent Bulb Current

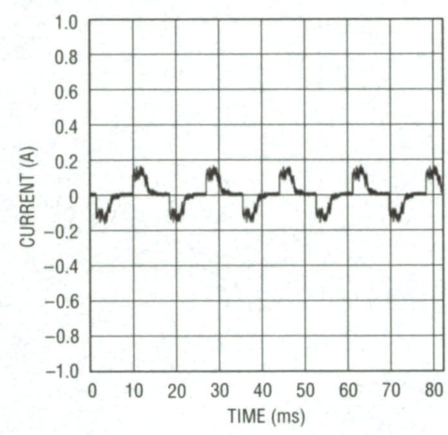

Figure 5. 4W LED Bulb Current

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Circuits protect outputs against overvoltage

Dimitri Danyuk, Kiev, Ukraine

In test-and-measurement applications, you must provide overvoltage protection for the output terminals of amplifiers, power supplies, and similar components. The conventional way to accomplish this task is to add series resistors with the output node along with the clamping diodes to power-supply rails or other threshold voltages (**Reference 1** and **Figure 1**). This resistor significantly reduces current-output capability and

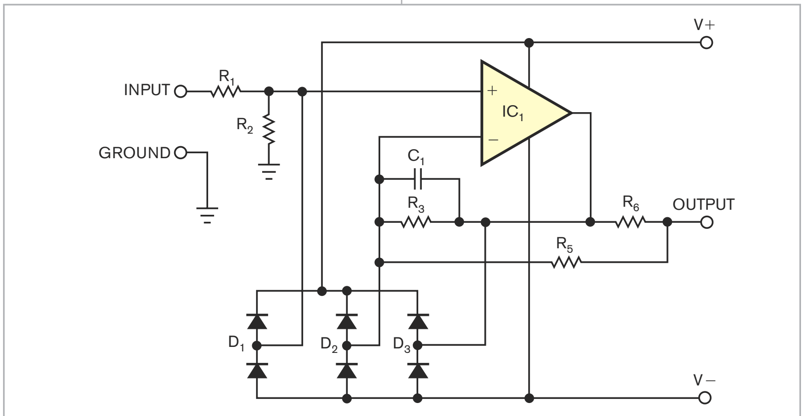

Figure 1 The conventional way to provide overvoltage protection is to add series resistors with the output node along with the clamping diodes to power-supply rails or other threshold voltages.

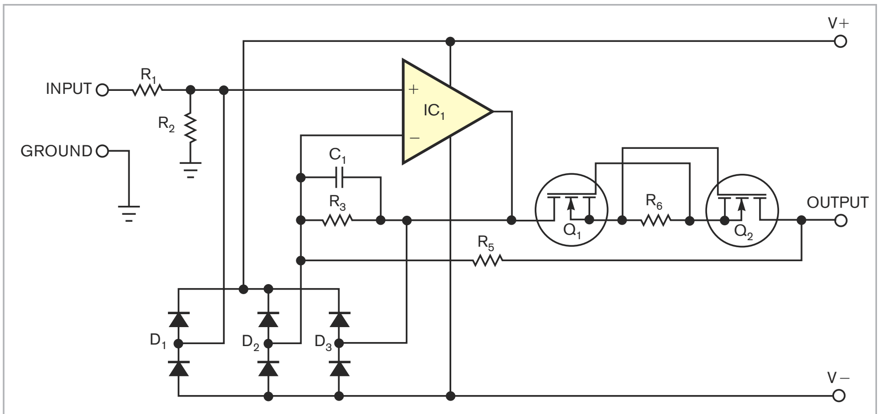

Figure 2 This circuit works as a bipolar-current source when the voltage drop across source resistor R_6 becomes larger than the gate-threshold voltage of depletion-mode MOSFETs Q_1 and Q_2, thus limiting the current through clamping diodes.

the output-voltage swing with low-resistance loads. The alternative approach is to use fuses or other current-limiting devices, which precede these clamps' high energy-absorption capability. The circuit in **Figure 2** works as a bipolar current source when the voltage drop across source resistor R_6 becomes larger than the gate-threshold voltage of depletion-mode MOSFETs Q_1 and Q_2, thus limiting the current through the clamping diodes (**Reference 2**). The drawback of this approach is high power dissipation on series components during the overload condition.

A reasonable approach disconnects the amplifier-output node from the output terminals for the period when the overload voltage exists on output terminals. Engineers for decades have used such serial disconnection by means of electromechanical relays in audio power amplifiers but for a different reason: loudspeaker protection. SSRs (solid-state relays), including optoelectronic, photovoltaic, OptoMOS, and PhotoMOS devices, suit the task

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of load disconnection at moderate current levels because of galvanic isolation between the control and the load pins (**Reference 3**).

The series-protection circuit of **Figure 3** disconnects the amplifier-output terminal using a series-connected, high-voltage SSR. Raising the output voltage above the positive-reference-voltage or below the negative-reference-voltage threshold causes either the IC_2 or the IC_3 comparator to change its output state and turn off SSR IC_4 through AND logic element IC_5. **Figure 4** shows the simple circuit realization of this approach.

The circuit in **Figure 4** requires only a couple of external components to use an SSR for output-overvoltage protection. Rising overvoltage turns off both transistors in IC_2, interrupting current flow through the control LED of IC_3. Relay IC_3 opens, protecting the amplifier and clamping diodes. The circuit was tested with a handful of Clare, Matsushita Electronic Works, and Panasonic (www.clare.com, www.naisis.co.jp/english, www.panasonic.com) SSRs with and without internal current protection. The power-supply rails are $\pm$15V; R_{10}, R_{11}, and R_{12} set the triggering levels and are equal to $\pm$16V. Omitting R_{11} shifts the triggering levels to $\pm$14.5V. The SSR turn-off delay in protection-circuit operation is 100 to 200 μsec for relays with 0.5V overvoltage protection and becomes slightly shorter with higher overvoltage. Note that the peak current through clamping diodes can be rather high with low-on-resistance SSRs. **EDN**

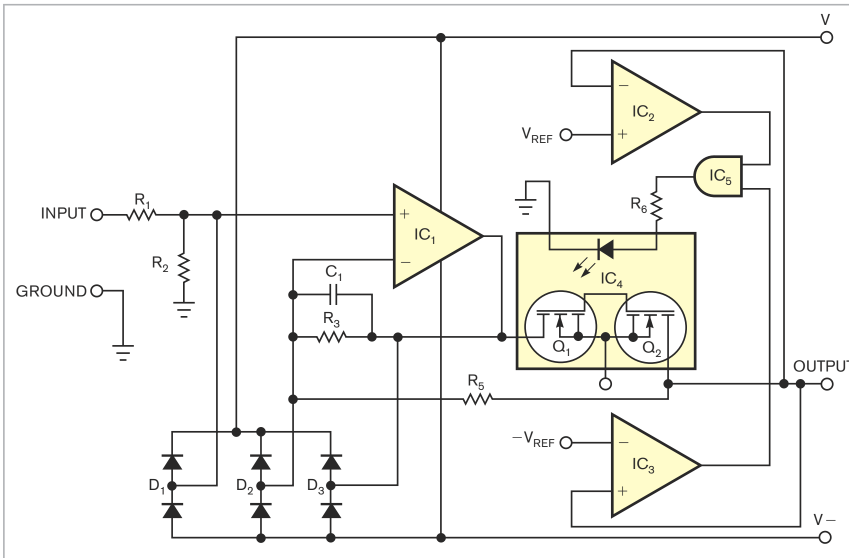

Figure 3 This series-protection circuit disconnects the amplifier-output terminal using a series-connected, high-voltage SSR.

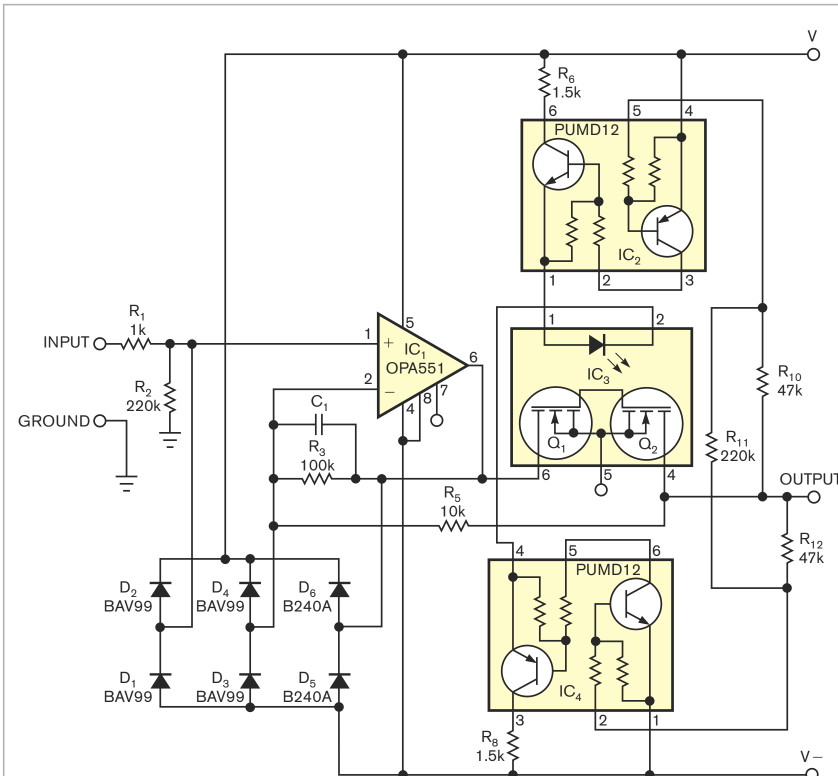

Figure 4 This circuit requires only a couple of external components to use an SSR for output-overvoltage protection.

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CPLD connects two instruments with half-duty-cycle generator

Yu-Chieh Chen and Tai-Shan Liao,
National Applied Research Laboratories, Hsinchu, Taiwan

When synchronizing two instruments' signals, it is important to make sure that the receiver can latch the sender's synchronous signal. For example, a pulse generator generates synchronizing pulses while generating the main pulse signal. For the Avtek (www.avtekcorp.com) AV-1015B, the pulse generator's duty cycle is approximately 50 nsec at TTL with a 50Ω load. The goal of this Design Idea is to increase the pulse generator's high-level width to meet the triggering spec of a lock-in amplifier. The synchronizing pulse's frequency is 10 Hz to 102 kHz, which is the lock-in amplifier's frequency range.

Because the synchronizing pulse synchronizes to the main pulse, you must minimize any delay in calculating the lock-in amplifier's synchronizing input. And, because the user can change the frequency of the pulse train from the pulse generator, the synchronizing signal's frequency also changes. Therefore, you must make sure that the circuit properly calculates and generates the synchronizing signal, no matter how the user sets the output of the pulse generator.

Figure 1 shows the half-duty-cycle generator's algorithm. The CPLD first waits for the positive-edge trigger, then starts to count at a frequency of 60 MHz, and waits for the next positive-edge trigger. When the next positive edge comes, the synchronizing signal's period counting is complete. The counting value then gets saved in a buffer and divided by 2 to yield the value for half-duty-cycle generation.

In tests, the half-duty-cycle generator in this Design Idea worked over a frequency range of 2 Hz to 450 kHz. You can use this design not only in a pulse generator, but also in any synchronizing signal in which the pulse is too narrow for other system triggering. The half-duty-cycle generator fits into a CPLD, such as an Altera (www.altera.com) EPM570 with a 60-MHz system clock and an MM74-HCT244 buffer to output a TTL signal. **Listing 1** contains the program for the CPLD. **EDN**

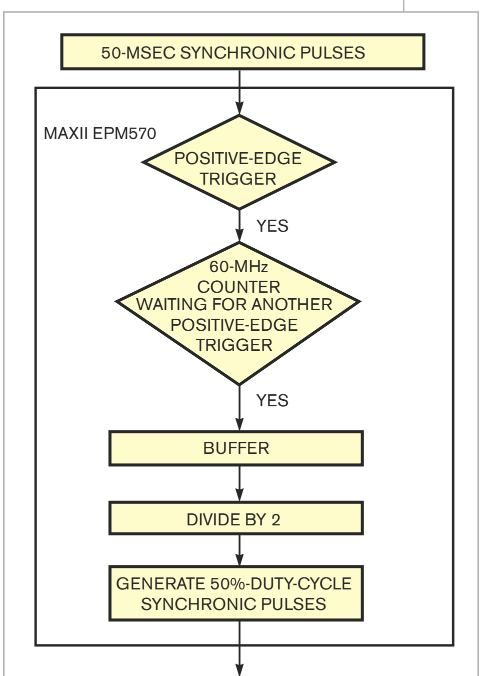

Figure 1 When programmed into a CPLD, this algorithm expeditiously generates a synchronizing signal at half the input frequency.

LISTING 1 GENERATING 50% DUTY CYCLE

```
module PulseDutyCycle  (
          input  iReset,
          input  iClk,
          input  iPPS,

          output  oSynPulse
         );

 reg   mOldPulse;
 reg    mState;

 reg   [25:0]  mCount2;
 reg   [25:0]  mCount1;
 reg   [25:0]  mCount;     //67108864


 always @( posedge iClk )   //trigger by 60MHz clock
 begin
  if( !iReset )
  begin
  case( mState )
   1'd0:
   begin
    if( mOldPulse==0 && wClk==1 )  //postive edge trigger
    begin
     mCount     = 0;    //start to count
     mOldPulse   = wClk;
     mState    = 1;
    end
    else
    begin
     mCount       = mCount  +  1;
     mOldPulse   = wClk;
     mState    = 0;
    end
   end
   1'd1:
   begin
    if( mOldPulse==0 && wClk==1 )
    begin
     mCount2   =   (mCount+1)/2;    //add the first flag count,
the first count done,and divide by two
     mCount1    = mCount;          //save the total end count
     mount    = 0;
     mold Pulse  =  walk;
     mutate    =  0;
    end
    else
    begin
     mount    = mount  +  1;
     mold Pulse  =  walk;
     mutate    =  1;
    end
   end
  encase
  end

  else if( ((mold Pulse==0)&&(walk==1)) || (mount>=mCount1)
  begin
   mount    = 0;
   mold Pulse  = walk;
  end

  else
  begin
   mount    = mount  +  1;
   mold Pulse  = walk;
  end
 end

 assign oSynPulse  =  (mCount<=mCount2)? 1:0 ; //Output the
cycle pulse

endmodule
```

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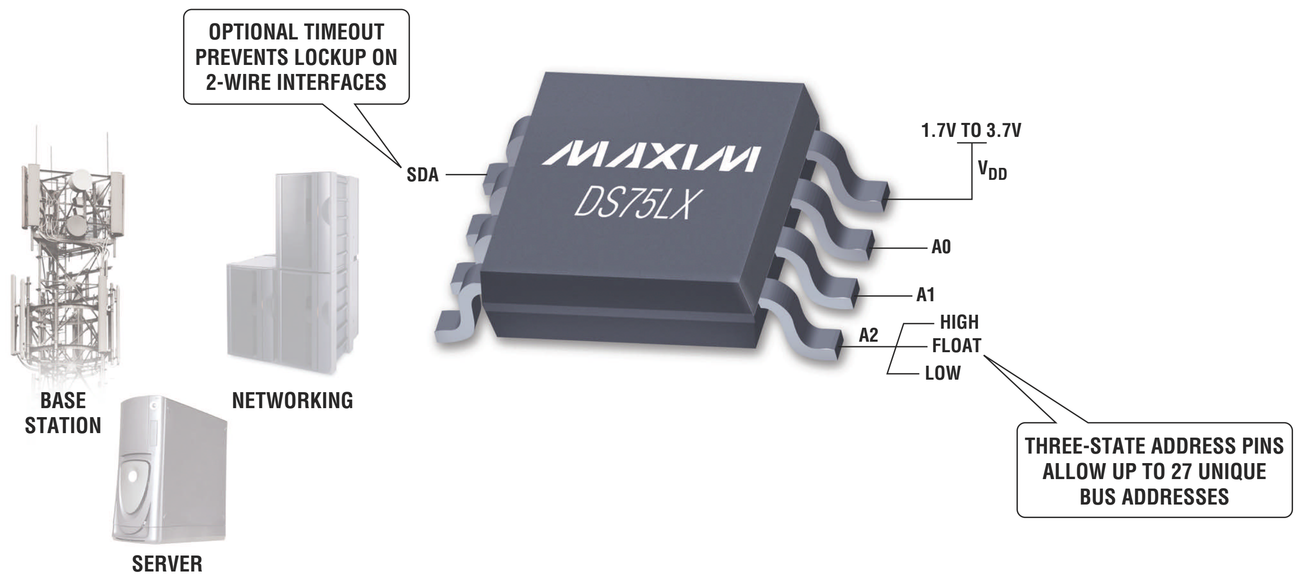

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DS75LV	1.7 to 3.7	8	✔	8-µSOP, SO
DS1775	2.7 to 5.5	1		5-SOT23
DS75	2.7 to 5.5	8		8-µSOP, SO

SMBus is a trademark of Intel Corporation.

†1000-up recommended resale. Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates. Not all packages are offered in 1k increments, and some may require minimum order quantities.

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Achieve simple IR-data transmission from a PC's serial port

Andreas Grün, Wedemark, Germany

Often, you need to transmit a couple of bits or bytes of data to a microcontroller without a direct cable connection. One simple way to achieve this goal is to use a widely available IR receiver, such as a TSOP17xx or similar receiver from Vishay (www.vishay.com) that finds use in IR-remote-control applications, such as TVs and VCRs. These devices are easy to implement because they require no external parts. These receivers usually work with a pulsed 38-kHz carrier and include an amplifier, automatic gain control, and a demodulator.

The main problem for simple applications is building the transmitter, which requires a 38-kHz start-stop oscillator, additional supply voltage, and modulating pulses in the millisecond and submillisecond range. These factors are difficult to control with PC operating systems. On the other hand, a PC's serial port at a standard transmission rate of 38,400 bps can generate precise bursts of 38.4-kHz data with a simple frequency doubler and two IR LEDs (**Figure 1**). When transmitting bytes with an alternating zero/one pattern (hex 55), each hex-55 byte generates a burst of 18 pulses, adding the start and stop bit, and consecutive bytes can generate longer pulses.

The receiver needs pulse trains ranging from 10 to 70 pulses with approximately equal pauses between them; you can easily meet these requirements with this setup. You can generate short pauses by sending hex-0 bytes, although two pulses will transmit for each byte because of the start and stop bits. However, the receiver eliminates these pulses. Stopping the transmission for a time can generate longer pauses. You must occasionally insert longer pauses, depending on the receiver you use. You can achieve data transmission by using short and long bursts and an appropriate protocol.

The circuit in **Figure 1** forms a high-pass filter with the output impedance of the serial port and the capacitor. The positive pulses drive one IR LED; the negative pulses drive the other. Both should point to the receiver. PC ports usually provide a maximum current of 5 to 20 mA and a voltage of ±15V, thus having an output resistance in the low-kilohm range. A current-limiting resistor is usually not necessary. A value of 1 to 10 nF for the capacitor works in most cases. The receiver is tolerant. You need to adjust the capacitor's value for non-PC ports, such as the microcontroller, which have lower impedance. In practical applications, you can reliably achieve a transmission distance of 2 to 4m with a peak LED current as low as 5 mA if you point the LEDs at the receiver. A sample program for the PC is available at the *EDN* version of this Design Idea at www.edn.com/071011di1. EDN

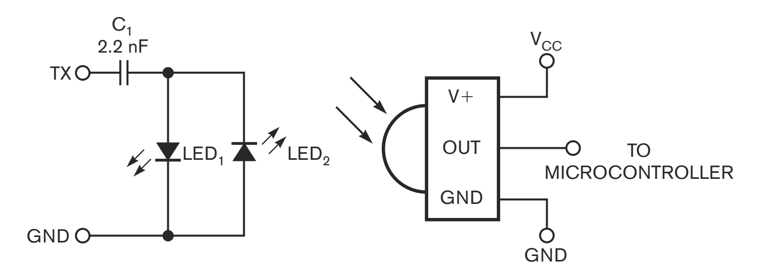

Figure 1 By sending appropriate hex values to a PC's serial port, this circuit generates precise bursts of 38.4-kHz data.

Circuit limits dV/dt and capacitor inrush at regulator turn-on

W Stephen Woodward, Chapel Hill, NC

Unusual design constraints sometimes reveal the unfriendly side of everyday components and circuits. A case in point is the design of power-supply-regulation circuitry in which the primary power source has an absolute current-limit specification, such as spacecraft photovoltaic, or "solar," panels and radioisotope-thermoelectric generators. Such applications require that you pay scrupulous attention to strict control of current consumption, including transient-current consumption, and infrequent consumption spikes, such as those that typically occur on power-up. The problem is that current-limited primary-power sources can suffer catastrophic voltage droop and shutdown in response to momentary overcurrent faults, even when the fault is brief. Common causes of such faults are the current spikes that charge the regulator output's decoupling capacitor.

Unless the current limit of the regulator clips the resulting spikes, the spikes are equal to the regulator's output-voltage rate of rise multiplied by the sum of the parallel output capacitances: $I_{MAX}=dV/dt \times C_{OUT}$, where I_{MAX} is the maximum current, dV/dt is a differential in voltage with respect to a differential in time, and C_{OUT} is the output capacitance. The math suggests that the best strategy for limiting the regulator's turn-on maximum current is

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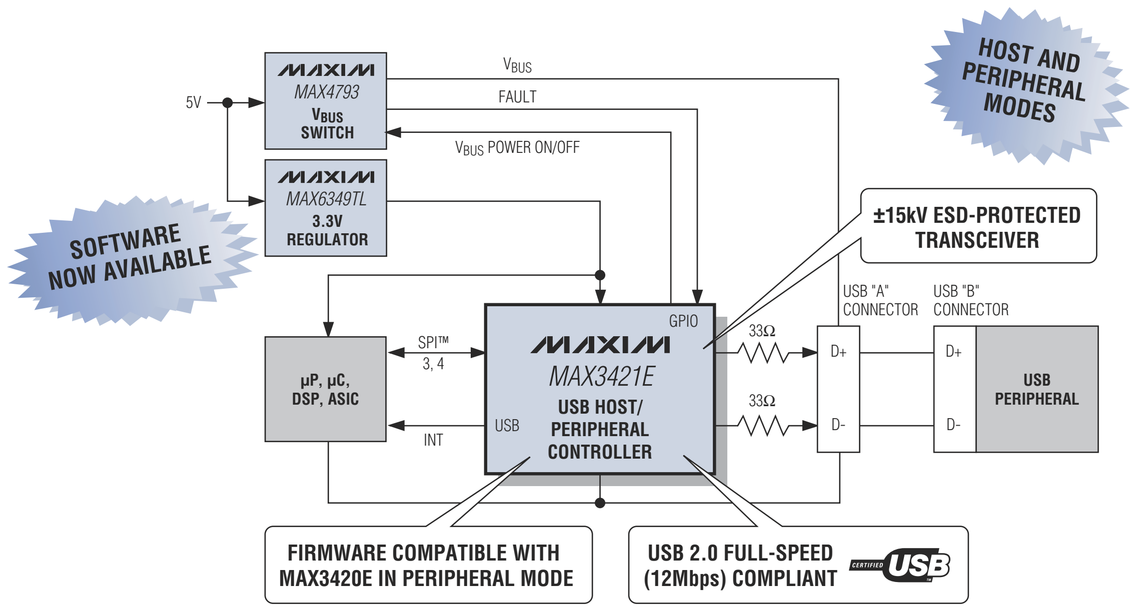

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to limit dV/dt. The circuit in **Figure 1** relies on this trick and works with industry-standard adjustable linear regulators, such as the popular low-dropout LM2941.

The basis of the dV/dt-limiting technique comprises the six added components: R_3, R_4, C_T, D_1, D_2, and Q_1. On power-up, the control current through R_3, C_T, and D_2 delays the rise of the output voltage and thus prevents excessive maximum-current transients.

Here's how it works. When V_{IN} is on and Q_1 is off, current through R_3, C_T, and D_2 pulls the adjust pin of the regulator to the reference. This action limits V_{OUT}'s dV/dt to the rate of C_T charging through the series resistance, $(R_3+R_1R_2/(R_1+R_2))$, and thereby limits I_{MAX} to any desired value using the design **equations** $R_3=(V_{IN}-V_{REF}-1)/V_{OUT}$, $R_4=<20R_3$, and $C_T=C_{OUT}V_{OUT}/(I_{MAX}(R_3+R_1R_2/(R_1+R_2)))$. For example, given the circuit constants in the **figure** and assuming $C_{OUT}=100$ µF, dV/dt=2500V/s, and $I_{MAX}=0.25$A. At the end of the modified power-up sequence, D_1 and D_2 decouple the dV/dt circuit from the regulator's feedback network, preventing the coupling of ripple voltages from the input voltage into the output voltage. **EDN**

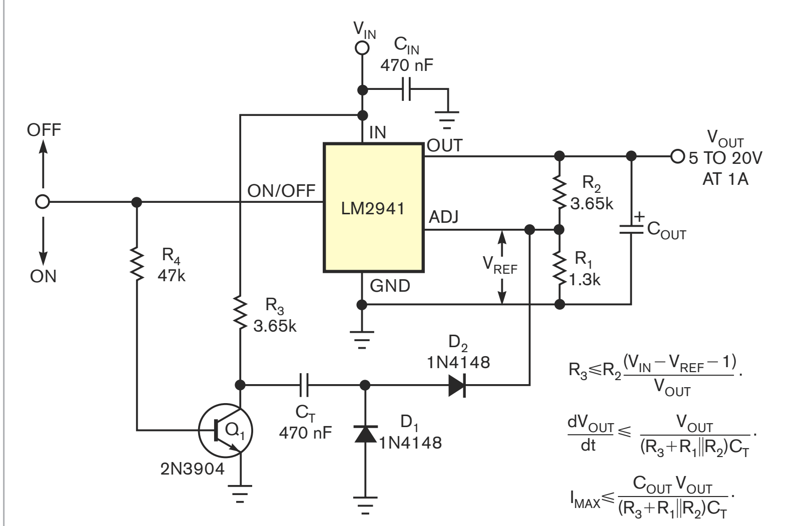

Figure 1 On power-up, the control current through R_3, C_T, and D_2 delays the rise of V_{OUT} and thus prevents excessive I_{MAX} transients.

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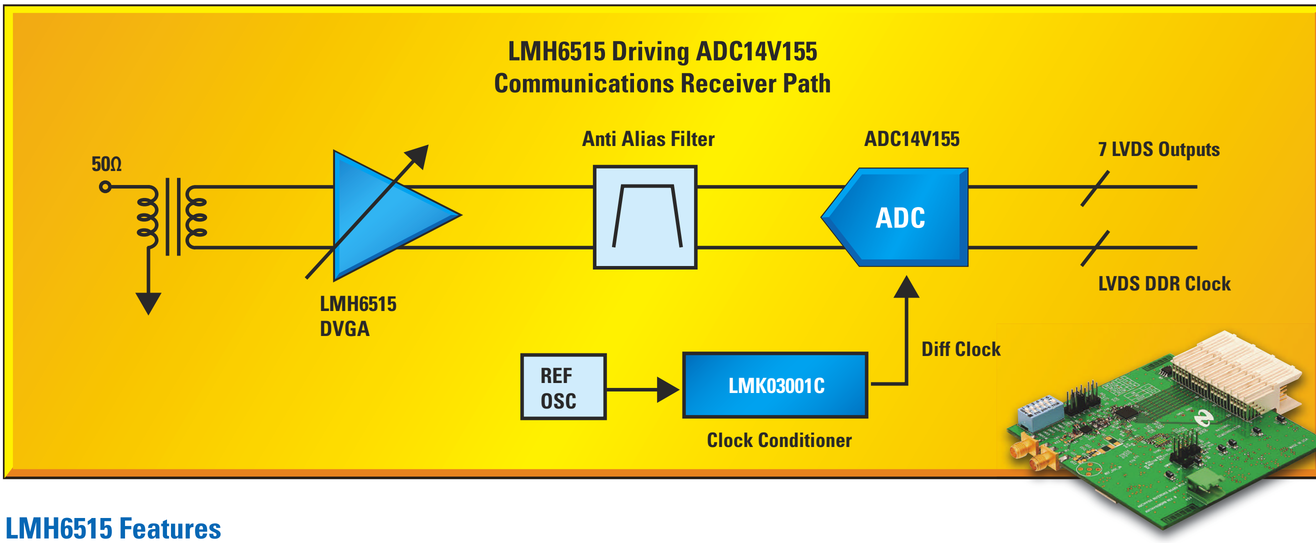

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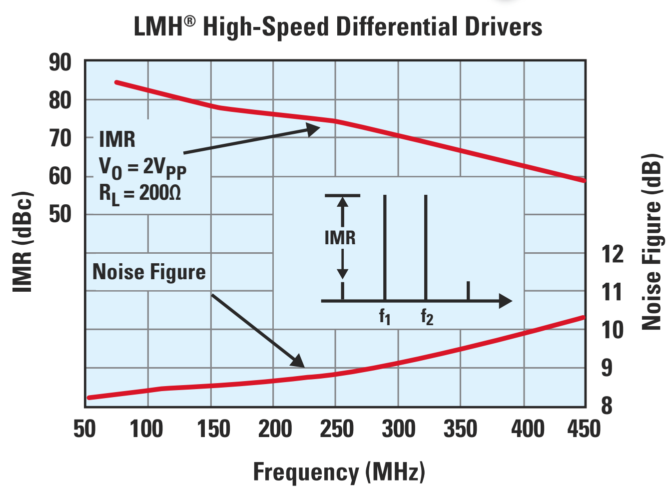

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LINKING DESIGN AND RESOURCES

Microcontrollers boost local distribution business in China

Microcontrollers are gaining widespread attention in China; increased consumer demand for intelligent features in consumer and communications products is fueling this interest.

Microcontrollers are showing up in everything from rice cookers to joysticks. Although that proliferation opens up opportunities, it also makes it challenging for Chinese vendors to deliver the right reference designs and design support.

Chinese distributors and independent design houses have rushed to fill the void. The partnership is synergistic; design houses have product knowledge, and distributors provide sourcing expertise.

CEASC (China Electronics Appliance Shenzhen Co, www.ceacsz.com.cn), a Chinese distributor with a franchise for Freescale microcontrollers, is a case in point. The company, which also has franchises for IDT, National Semiconductor, Zilog, Catalyst Semiconductor, Montage Technology, and AVX/KY, among other companies, has positioned itself as a provider for Chinese OEMs. Consequently, those turnkey systems use major lines that contributed to CEASC's revenue. According to Xun Liu, a vice president at CEASC, 80% of the company's revenue comes from design wins.

Local Chinese distributors started getting attention from international suppliers because of the diverse demand in China and increased design capability associated with the distributors. International suppliers are using international distributors to track transferred business to Chinese and Taiwanese distributors to serve Taiwan-based companies in China. Local distributors target local customers because of social networking and cultural concerns.

Though many consider Chinese distributors weak at supply-chain management, distributors *do* know how to serve their customers. One facet of that relationship involves technical support, which is why CEASC wants to be a provider rather than a trader. The company received its ISO9000 certification to improve its quality-control capability.

Based on research by China Outlook Consulting, orders by Chinese distributors accounted for 52% of China's distribution in the total market, and international distributors took 13% of local-order business in China.—**Amy Wang, Contributing Editor**

GREEN UPDATE

KOREA ROHS COMBINES EU ROHS, WEEE, ELV

Korea has set its own version of ROHS (restriction of hazardous substances) rolling with its Act for Resource Recycling of Electrical and Electronic Equipment and Vehicles.

The Korean government passed the act in April; members of the electronics-supply chain are calling the act Korea ROHS because of its similarities to EU (European Union) ROHS. But the regulation doesn't stop at just restricting substances.

Korea's law is broad and includes electrical and electronic equipment and parts, as well as automobiles. Although industry officials are dubbing it a member of the ROHS family, the act also has similarities to the EU's ELV (end-of-life-vehicles) directive, because of its conditions for automobiles, and the EU's WEEE (waste-electrical-and-electronic-equipment) directive, because of its recycling initiatives.

Broad as the directive may be, Korea's Ministry of Environment seemingly aims to keep it consistent with directives of the EU, including criteria for substance restriction, type, and concentration. The act also allows for exemptions for materials with no known substitute that you cannot remove from product design. The compliance date for Korea ROHS is Jan 1, 2008.

OUTLOOK

NAND GROWTH AHEAD

Research from Semiconductor Partners (www.semiconductorpartners.com) points to the computing segment as the driver behind NAND-flash memory's expected shipment and gigabyte-consumption growth.

NAND prices were flat to slightly up from March to the end of August, in part due to excitement from the NAND-based iPhone's June debut. Overall 2007 NAND revenues of $13.5 billion will show an increase of more than 15% from 2006, according to the company. The company further forecasts that 2007 NAND-unit shipments will increase 86% compared with last year, and 2007 gigabyte consumption will grow 217% year over year.

"Computing will grow at an astounding 55.7% CAGR [compound-annual-growth rate] from 2006 to 2011 and will account for nearly two-thirds of the NAND market by 2011," says Adrienne Downey, director of memory research at Semiconductor Partners.

The company expects NAND supply to remain tight in the near term; however, expect manufacturers to add a massive amount of NAND capacity over the next 18 months to help meet demand. The company expects 8 Gbits, the dominant density in 2007, to continue to be a top density through 2009.

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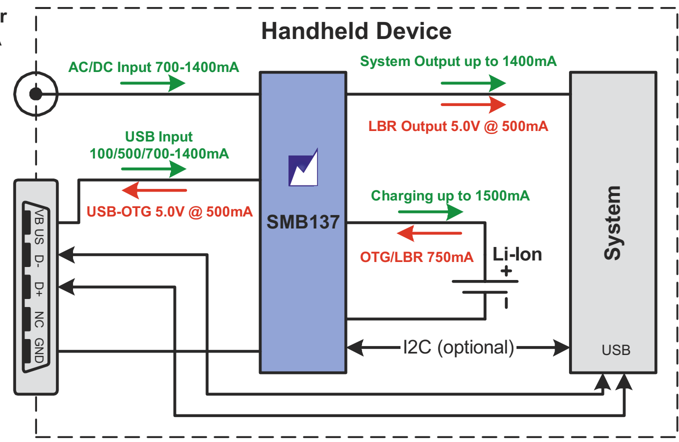

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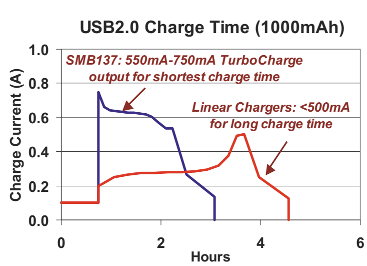
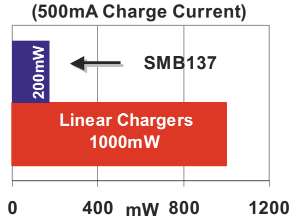
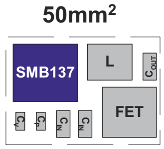


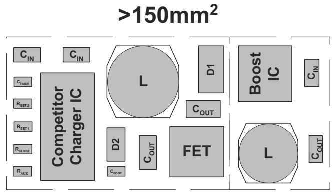


8 components
$50mm^2$



Summit SMB137
Charger + CurrentPath + OTG

19 components
$>150mm^2$



Competition's Charger + "PowerPath"

OTG "Extra Components"

*Patent(s) pending

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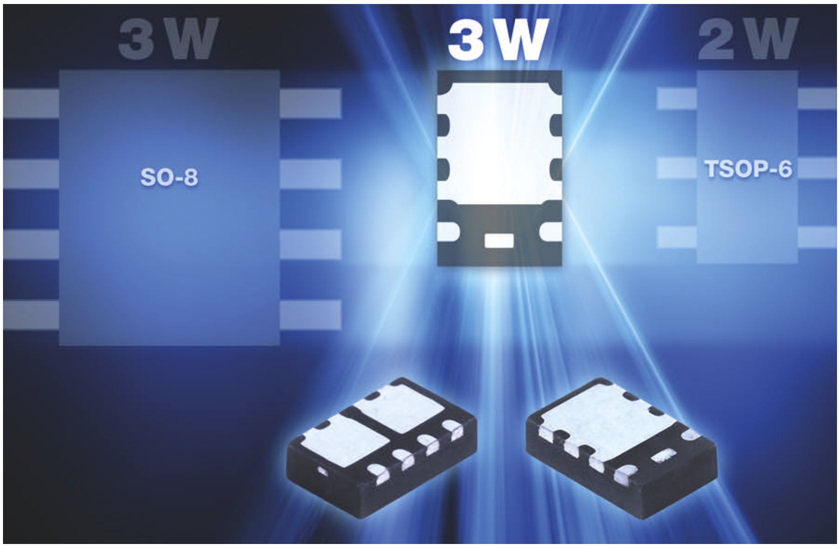

P-channel power MOSFETs come in PowerPAK ChipFET packages

Providing a 3×1.8-mm footprint, the seven P-channel MOSFETs in a PowerPAK ChipFET package feature a 75% lower thermal resistance, a 33% smaller footprint, and a 23% thinner height profile than those in a TSOP-6 package. The devices also feature 3W power dissipation—equal to that of the SO-8 package. Rated for 3°C/W junction-to-case thermal resistance, the devices feature a 0.021Ω maximum on-resistance in a 20V drain-to-source P-channel, single-channel device and 0.064Ω in a dual-channel device. The PowerPAK ChipFET MOSFETs cost 20 cents (100,000).

Vishay Intertechnology, www.vishay.com

Audio-amplifier transistors feature enhanced thermal stability

Aiming at audio amplifiers in home and professional markets, the Darlington transistor series features a high safe-operating area. The STD01N/P and STD02N/P transistors provide a built-in thermal-compensation diode on the same die, eliminating a delay for thermal-compensation operation and the delay between thermal sensing at the heat source and response at the compensation area. The devices achieve higher power levels by using decreased thermal resistance, making them suitable for applications requiring enhanced thermal stability. Available in a TO-3P package, the STD01N/P and STD02N/P cost $1.50 and $1.70 (1000), respectively.

Allegro, www.allegromicro.com

Digital transistors have tiny packages

The NPN FJY30xx and the PNP FJY40xx transistor series require no external resistor. These 200-mW digital transistors integrate an external resistor-bias network. Measuring 1.7×0.98×0.78 mm, the transistors come in SOT523F housing. The FJY30xx and FJY40xx series cost 3.7 cents (1000).

Fairchild Semiconductor, www.fairchildsemi.com

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LOOKING AHEAD

TO THE INTERNATIONAL SOC CONFERENCE

Commencing Nov 7 in Newport Beach, CA, this two-day, 5-year-old conference is attracting an increasingly interesting set of keynotes and technical papers. Among this year's keynote speakers, Jeff Parkhurst, academic-research-programs manager at Intel, will discuss tera-scale computing, complex SOC (system-on-chip) design, and Moore's Law. Rob Rutenbar, professor of electrical and computer engineering at Carnegie Mellon University (Pittsburgh), will discuss the statistical analyses that modern finance and risk analysis employ and their applicability to the problems of closure in SOC design. Panels will examine the challenges of wireless SOCs, directions in SOC architecture, and the future—if any—of structured ASICs.

LOOKING BACK

TO ASK "WHO NEEDS GPS?"

A military computer enables a vehicle operator to determine his exact position, as well as how to reach a designated position and return. Operators set the computer, which was jointly developed by the Army Engineering R&D Lab and Ford Instruments, by feeding in map coordinates for present and desired locations. The vehicle's gyro compass and speedometer or odometer cable provide continuous input, and the computer generates a continuous display of vehicle heading, heading to destination, and distance to destination. The computer compensates automatically for any deviation resulting from detours.

—*Electrical Design News*, October 1957

LOOKING AROUND

AT SHRINKING DRAM PRICES ... AGAIN

According to the analysts, after a recovery that lasted all of three months, DRAM prices are again on the decline. Of course, this news is bad for the few companies that dominate the DRAM business. But what does it say to the rest of us when such a technically complex, capital-intensive product can be in chronic oversupply? For one thing, it warns that there are no powerful market drivers out there to soak up the world's huge semiconductor-manufacturing capacity. Another point to ponder is that technological sophistication is no longer a market differentiator. It is no longer impractical to duplicate even a highly complex technology. Other factors, such as detailed applications knowledge, intimate relations with systems vendors, or just plain luck are necessary to earn margins in today's world.

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